

# COMPUTER SYSTEMS

## FACULTY

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## FPGAs can finally adapt without external control

Ever since the introduction of Field-Programmable Gate Array (FPGA) technology in the mid 80's, people have imagined computers that could evolve and adapt to changing conditions without requiring external assistance. That dream has come closer to reality as ECE researchers have demonstrated the first known instance of a system changing its own hardware in a non-trivial fashion while continuing to run.

A team in the Configurable Computing Laboratory (CCM) has demonstrated an embedded system that is able to interactively implement new circuits inside itself or remove or reconnect existing circuits. The system was developed by Neil Steiner, a Bradley Fellow and Ph.D. candidate, working with his advisor, Peter Athanas.

By folding low-level design tools into a demonstration system, the team has made it possible for computers to participate in their own design. "If our system finds defects within itself, it can simply avoid using the damaged resources," Steiner said. "This capability is much more cost-effective than throwing away large, but imperfect chips."

Internal modeling and design tools also allow the system to function at a higher level of abstraction than previous FPGA systems. Instead of requiring a configuration bitstream that supports a

specific FPGA model, the proof-of-concept system can accept circuit netlists in the widely popular EDIF format. These circuits are then placed, routed, configured, and connected to other circuits inside the system, without interrupting its operation. The same EDIF netlists can be used for any device in the same FPGA family, which ensures that designs remain more portable.

The current research falls within a proposed roadmap for autonomous computing systems—systems that are able to function more independently and assume responsibility for their own resources and operation, according to Steiner. The next step is to include a synthesizer within the system, so that it can accept behavioral circuit descriptions in high-level languages like VHDL or Verilog. "The most ambitious levels on the autonomy roadmap describe systems that can adapt to changing conditions and even learn from experience, a prospect that is not as far-fetched as it sounds," he said.

Steiner credits his Bradley Fellowship and support from Xilinx, the leading FPGA manufacturer, in enabling his research to push the envelope to show what can be accomplished with current technology. "FPGAs have taken on important and well-deserved roles in modern systems, but we have shown that the early dreams are still viable," he said.

# Wires on Demand: AIDING THE USE OF FPGAS IN SDR

**A** CpE team is creating middleware that allows software applications to easily use a dynamically loaded library of functions implemented in FPGA hardware. The “Wires on Demand” technology will enable greater use of FPGAs in software-defined radio (SDR) applications.

“FPGAs are ideally suited to the DSP requirements of software radios,” said Cameron Patterson, who, with Peter Athanas, serves as a faculty member on the project. “However, it is difficult to change SDR waveforms at run time,” he said. In current reconfigurable approaches, the inter-module communication structure usually remains fixed, which in software-defined radio applications, limits logic and routing resource efficiency.

Reconfigurable applications development is daunting for software radio designers, largely because inter-module communication requires low-level physical design, he said. “The designers must learn more about the FPGA architecture and tools than they ever want to

know. Run-time reconfigurable application design would be much easier if module communication circuitry was automatically synthesized.” Routing should be optimized between modules as much as within a module and avoid the use of buses, on-chip networks and crossbar switches with their significant latency, area and power overheads, he said.

With the team’s approach, choosing the module’s coordinates and completing connections to other modules are run-time operations. A library of relocatable partial bitstreams is created, which is used by the run-time system to complete application requests for instantiating and connecting modules.

Bradley Fellow alumni Mark Bucciero and Jonathan Graf, both of Luna Innovations, are on the project, along with graduate students Kipp Bowen, Tim Dunham, Matt Shelburne, Jorge Suris, and Bradley Fellow Justin Rice. The project is sponsored by the Air Force Research Laboratory.

## ECE joins new NSF center for reconfigurable computing

**E**CE’s Configurable Computing Laboratory, directed by Peter Athanas, is part of a new NSF Center for High-Performance Reconfigurable Computing (CHREC, pronounced “shreck”).

The new center, headed by the University of Florida, includes The George Washington University, Virginia Tech, and Brigham Young University. CHREC is the nation’s first multidisciplinary re-



search center in reconfigurable high-performance computing and is part of the NSF Industry /University

Cooperative Research Centers (I/CURC) program.

Including the university partners, about two dozen organizations comprise CHREC, ranging from the Air Force Research Laboratory to the Aerospace Corporation. Shawn Bohner of computer science is the Virginia Tech lead and co-director of the Center. Joining Bohner and Athanas are computer science faculty members Wu-Chun Feng and Francis Quek.



**e-Rug:** The e-Textile Laboratory is incorporating electronics into large surface areas, such as rugs and draperies. The rug prototype shown here was made with readily available electronic yarns and is being used as a testbed for tracking human gait. The rug lights up when the sensors are activated and has potential uses such as tracking people in low-visibility situations or directing traffic during evacuations.



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