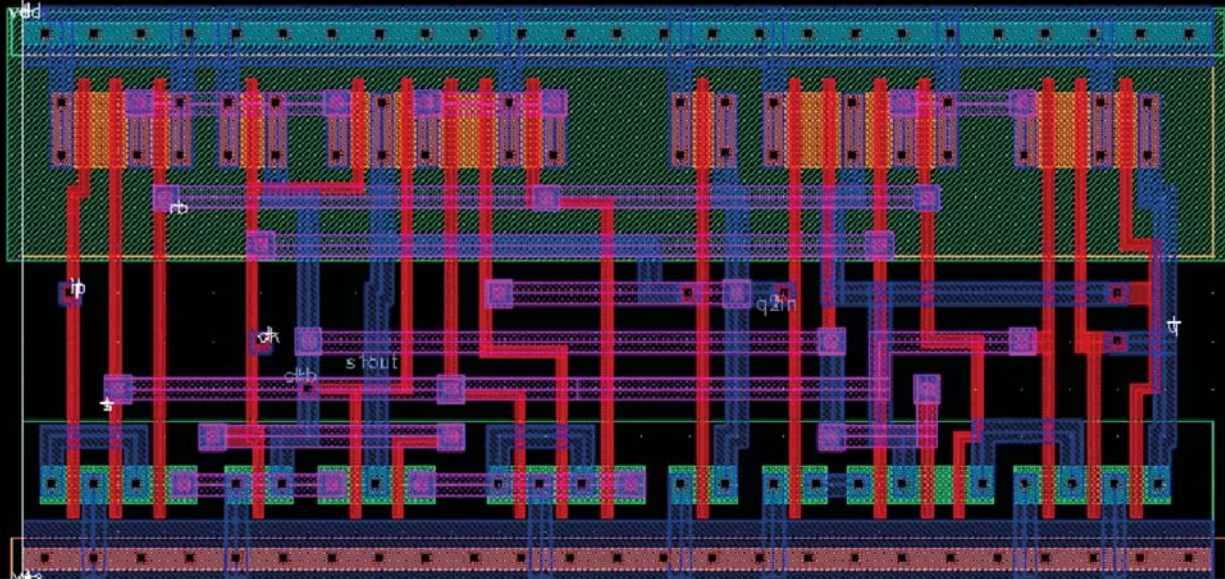


# VLSI & Design Automation

## FACULTY

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Virginia Tech's cell libraries for VLSI design have been used by more than 280 universities worldwide.

Image courtesy of Dong Ha

## Cell libraries boost academic VLSI research

**C**ell-based, VLSI design — the most widely used approach in system-on-a-chip design — relies on a building-block infrastructure with standard cell libraries. All aspects of VLSI benefit from standard cell libraries, including full custom design, automatic layout generation, physical design, logic synthesis, CAD tools, and testing.

An ECE research team, led by Dong Ha, has been developing and distributing a standard-cell library targeting the TSMC-0.25um, 2.5-volt CMOS process available via MOSIS, along with CAD tools for testing and the source code. The library has been used by more than 280 universities worldwide.

The team — VTVT (Virginia Tech for VLSI Telecommunications) group — recently has been awarded a \$421,337 grant

(subject to renewal for three years) from the NSF for further development of the library.

“Commercial library cells are the supplier’s proprietary information, and understandably, suppliers usually impose certain restrictions on the access and use of their library cells,” said Dong Ha, VTVT director. “Those restrictions on commercial library cells severely hamper academic VLSI research and teaching activities. This grant aims to address the problem so that academic researchers can freely exchange designs utilizing those library cells.”

Planned improvements include development of library cells for other processing technologies; development of RAM and ROM compilers and data converters; and provision of additional features and simulation libraries.

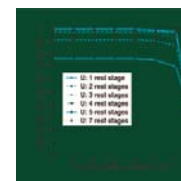
### Center for Embedded Systems in Critical Applications (CESCA)



[www.ee.vt.edu/~cesca/](http://www.ee.vt.edu/~cesca/)

The multidisciplinary center develops enabling technologies to support distributed decision-making among hundreds or thousands of networked computing nodes. Applications in healthcare, environmental monitoring, transportation, and business are the main focus of the Center. Director: Dong Ha.

### Formal Engineering Research with Models Abstraction, and Transformations Laboratory



<http://fermat.ece.vt.edu>

FERMAT investigates embedded system design methodology, verification, low-power design of embedded systems, high level modeling and synthesis, and CAD.

Director: Sandeep Shukla

# VLSI & Design Automation Overview

Research activities encompass the design, modeling, testing, and analysis of computational machines at all levels, including logic gates, integrated circuits, systems-on-a-chip (SoC), micro-architectures, and network architectures. Particular emphasis is on high speed and low-power VLSI design for software defined radios, analog, mixed-signal and RF design for ultra wideband radios, bio-microelectronics sensor design, nanotechnology architecture and design for computing, modeling of SoC, reliability and testability of digital hardware, computer-aided design for VLSI, and design methodology for embedded systems.

## MIT startup taps FERMAT for technology transfer.

Researchers from the FERMAT (Formal Engineering Research with Models, Abstraction, and Transformation) laboratory are working with an MIT-startup firm, Bluespec, Inc., to extend the features of the firm's Electronic Design Automation tools.

Bluespec's toolset, which is based on functional programming technology, delivers a high-level design and verification environment to current Verilog and VHDL designers of ASICs and FPGAs.

Gaurav Singh, a FERMAT Ph.D. student is working to develop low-power features for Bluespec's hardware compiler, and Hiren Patel, also a Ph.D. student, is helping Bluespec develop extensions that would enable SystemC-based designers to apply Bluespec's computation model. FERMAT director, Sandeep Shukla, will also work closely with the firm this summer.

## Proactive Research on Advanced Computer-Aided Testing, Verification, and Power Management Techniques

[www.proactive.vt.edu](http://www.proactive.vt.edu)

PROACTIVE focuses on state-of-the-art CAD algorithms for automatic testing, verification, and power management of large, high-performance system-on-a-chip (SoCs) and VLSI circuits. Director: Michael Hsiao



## Reliability of reconfigurable nanosystems

FERMAT researchers have been collaborating with the Los Alamos National Laboratory (LANL) to develop reliability analysis methodologies and tools for reconfigurable nanosystems.

As part of the DOE funded Reconfigurable and Adaptive Systems research project, Paul Graham from LANL's International, Space and Response (ISR) division has been working with ECE's Sandeep Shukla and Ph.D. student Debayan Bhaduri.

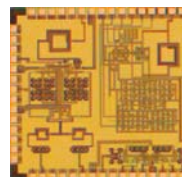
The effort has led to the development of a number of tools, including NANOLAB — a tool for designing and analyzing commercial-off-the-shelf nanoscale CMOS systems. Tools for designing and analyzing molecular memories and molecular reconfigurable systems have also been developed.

Bhaduri has also been working with Heather Quinn from the ISR Space Data Systems, on transitioning these tools to the different projects within ISR. Quinn and Bhaduri are developing an improved reliability and performance analysis system called STARS for nanoscale computational structures. STARS integrates seamlessly with the current hardware design flow. These tools are being applied in image and signal processing systems critical for the threat reduction and nonproliferation missions of ISR.

The effort's long-term goal is an unified framework for (1) designing reliable, high performance and power-efficient systems from unreliable nanodevices, and (2) developing computing architectures for novel non-silicon nanodevices such as carbon nanotubes and single electron transistors. Such a framework will help the development of complex nanoscale sensor systems — systems that will be very critical in national and homeland security. Further, with the development of the Center for Integrated Nanotechnologies (CINT) jointly between LANL and Sandia National laboratories, such a nanoscale design framework will impact a number of future applications. Further information on this research project is available at [www.rasr.lanl.gov](http://www.rasr.lanl.gov) and [www.fermat.ece.vt.edu](http://www.fermat.ece.vt.edu). LAUR-06-1628

## Virginia Tech VLSI for Telecommunications (VTVT)

[www.ee.vt.edu/~ha/research/research.html](http://www.ee.vt.edu/~ha/research/research.html)



VTVT laboratory focuses on low-power VLSI design for software defined radios and multimedia applications, analog, mixed-signal and RF design for ultra wideband radios, nanotechnology design for computing, and bio-microelectronics sensors.

Director: Dong Ha