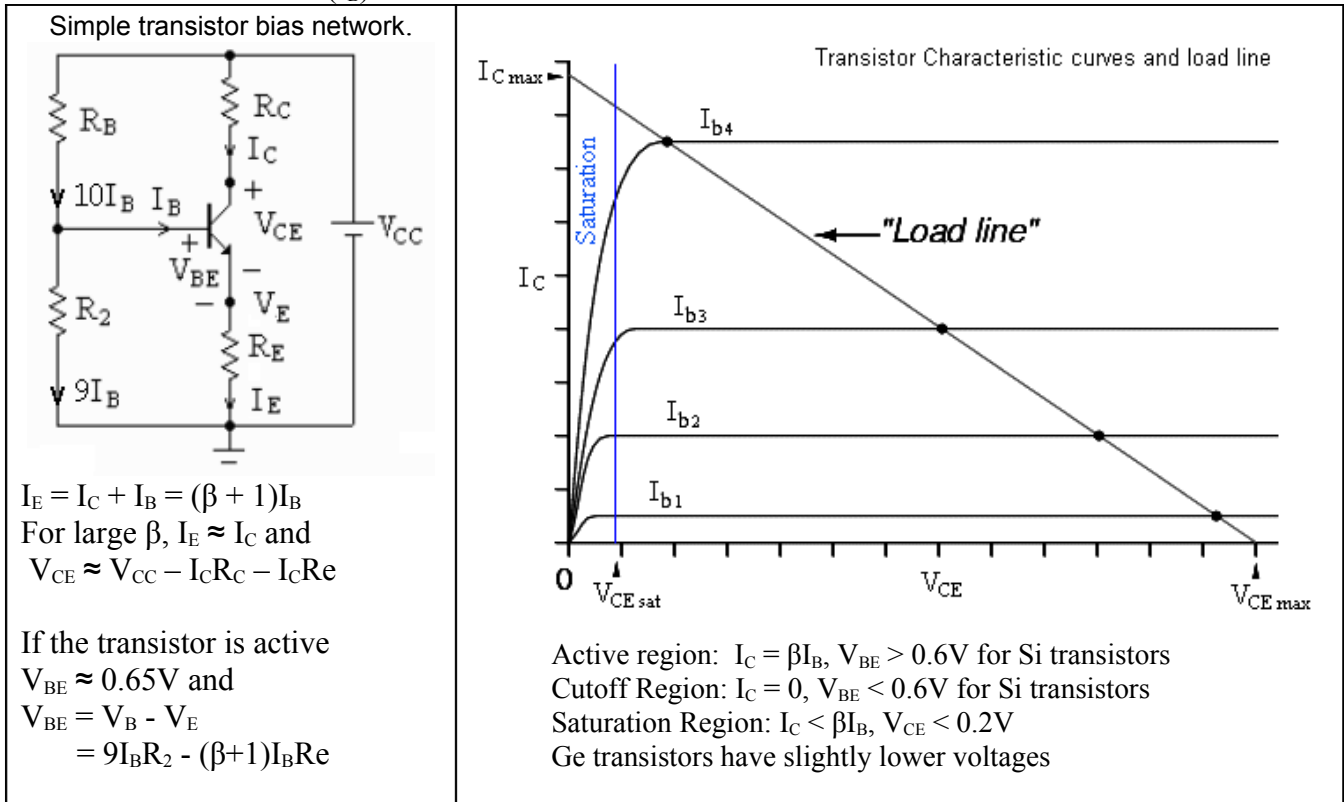


ECE 3254 PreLab 7 notes

Edited 10-08-2009

The 2N2222 or PN2222 Silicon Bipolar Junction Transistor (BJT) is widely used for general purpose amplifier and switch applications. DC current gain (β) for this NPN transistor is typically between 100 and 200 and the gain bandwidth product (f_T) is around 300 MHz. Numerous data sheets can be found using your favorite search engine.

A set of characteristic curves provides a picture of what we can expect from a working BJT. Each curve shows how the collector current (I_C), varies with the Collector-Emitter voltage (V_{CE}), for a specific fixed value of the Base current (I_B).



The circuit Load Line is a plot, on the transistor's characteristic curves, of I_C vs. V_{CE} for all base currents. The quiescent point (Q point) is the static location on the load line that corresponds to the transistor bias point. All transistor operation will lie on the load line - any change in I_B will move the operating point diagonally along the load line.

Note how $V_{CE\ max}$ occurs when $I_C = 0$ (cutoff region) and $V_{CE\ max} = V_{CC}$ when the voltage drop across R_C and R_E are $0V$. Similarly, $I_{C\ max}$ occurs in the saturation region when $V_{CE} = 0$ and current flow is only limited by R_C and R_E [$I_{C\ max} \approx V_{CC}/(R_C + R_E)$ because $I_e \approx I_C$ for large β].

Cutoff occurs when V_{BE} is too low to turn the transistor base-emitter junction on, so $I_C = 0$.

Active mode is the linear region, where the I_b curve is flat, is used for amplifier circuits. Power dissipation in the transistor must be kept below the transistor's rating.

Saturation occurs when I_C does not proportionally increase as I_B is increased ($I_C < \beta I_B$). For most silicon transistors, this is when $V_{CE} \leq 0.2V$. Transistors used for switching applications are toggled between Saturation and Cutoff.

Bias Circuit Design – suggested procedure

Use standard resistor values that are as close as possible to the values you need.

$I_C = 15\text{mA}$ (given)

I_B For $\beta = 150$ (typical for the 2N2222), $I_B = I_C / \beta = 15\text{mA} / 150 = 100\mu\text{A}$

V_E and R_e Select a value for V_E somewhere between 1 and 2V. Recommend: 1.5V for this experiment. For $\beta = 150$, $I_e \approx I_c = 15\text{mA}$. $V_E \approx I_C R_e$, solve for R_e .

Standard resistor values are **68Ω (1.02V)**, **82Ω (1.23V)**, **100Ω (1.5V)**, **120Ω (1.8V)**

(this is a rule of thumb - for bias stability you want 1 to 2 volts across R_e to compensate for differences in transistor β or changes in the transistor temperature.)

V_C Select a V_C somewhere between V_{CC} and V_E such as the midpoint $= (V_{CC} + V_E) / 2$ (the midpoint gives you the largest possible voltage swing)

V_B An active transistor has $V_{BE} \approx 0.65\text{V}$ so $V_B = V_E + 0.65$

V_{CE} $V_{CE} = V_C - V_E$

R_c Use ohms law to choose R_c so that $R_c = (V_{CC} - V_C) / I_c$ when $I_c = 15\text{mA}$

$R_c = (V_{CC} - V_C) / I_c$

Standard values are 220, 270, 330, 390, 470, 560, 680, 820, and 1K

R_1 For best bias regulation, the current through R_1 should be about 10 times I_B .

$V_{R1} = V_{CC} - V_B$. Using ohms Law, $R_1 = V_{R1} / 10I_B$

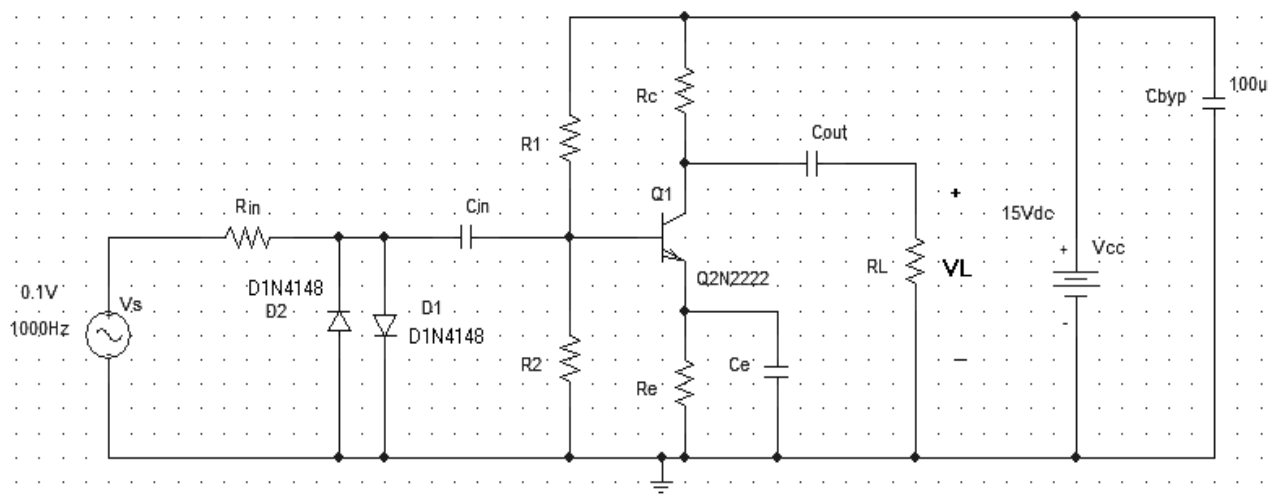
Standard resistor values are 8.2k, 10k, 12k, 15k, 18k, 22k

R_2 $I_{R2} = I_{R1} - I_B = 10I_B - I_B = 9I_B = 900\mu\text{A}$

Use ohms law to find $R_2 = V_B / I_{R2} = V_B / 9I_B$

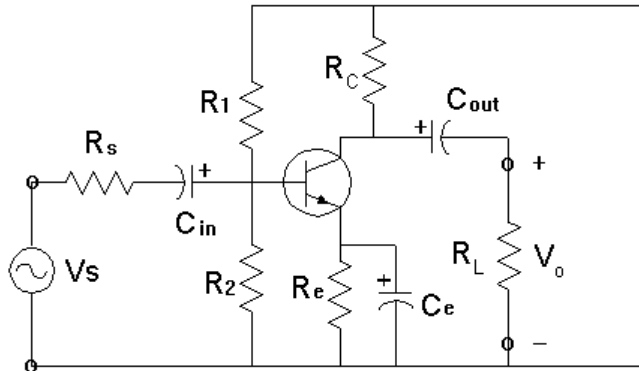
Standard values are 1.5k, 1.8k, 2.2k, 2.7k, 3.3k, and 3.9k.

AC Analysis

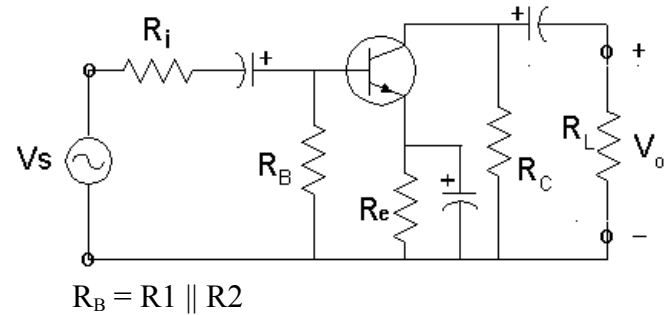


After the DC bias design has been completed, the AC equivalent circuit is obtained by recognizing that C_{byp} and the large filter capacitors in the power supply of the source (V_{CC}) are a short circuit to small signal AC. So V_{CC} in the original circuit above effectively connects R_b and R_c to ground. Also, the diodes only conduct if the input voltage is too high, so they are open for small signal inputs.

With V_{CC} shorted, the AC circuit becomes:

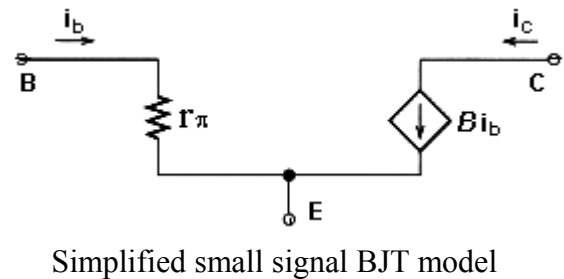
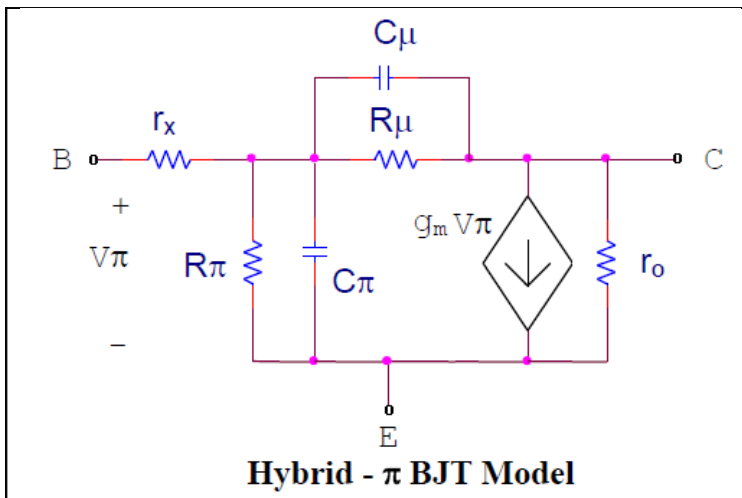


With some rearrangement of components, the AC circuit simplifies to:

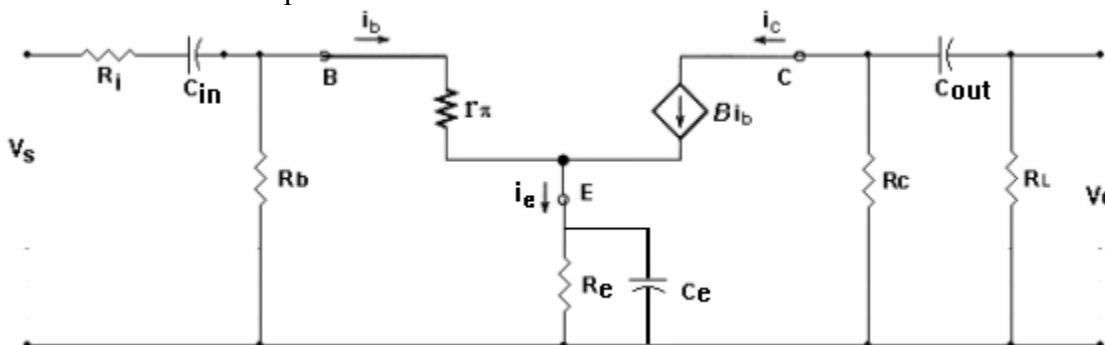


The Hybrid- π transistor model is accurate for high frequency circuit modeling, but it is overly complicated for the low frequency circuits used in the lab.

For low frequency (below 100kHz) circuits, we use the simplified model shown below right.



With the substitution of the simplified BJT model into the AC simplified circuit, the resulting AC circuit model for the entire amplifier circuit becomes:



r_{π} The model uses r_{π} for the AC base resistance where $r_{\pi} = \beta V_T / I_C$ ($V_T = 26\text{mV}$ from the standard diode equation mentioned in Lab 5).

For small signals, $r_{\pi} = \Delta V_{be} / \Delta i_b$, which is the slope of the I_B vs V_{BE} base “diode curve” at the transistor's DC bias point.

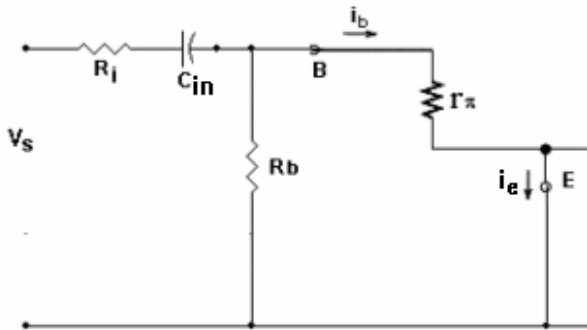
Finding the capacitor values

We want a low cutoff frequency of about 300Hz to eliminate noise from the 60Hz power line. C_e , C_{in} , and C_{out} each determine a cutoff frequency, and if they all have a cutoff at 300 Hz, the response would be down 9dB at 300 Hz (each capacitor will contribute -3dB at the cutoff). If we set each capacitor value so that its cutoff is 1/3 of the desired cutoff frequency, the effect of all three capacitor responses combined will produce a cutoff at about the frequency we want. Thus, **each capacitor should be sized to cut off at 100Hz.**

C_e Rule of thumb – for the common Emitter amplifier, you want C_e 's impedance to be $5\Omega < Z_C < 10\Omega$ at the the desired cutoff frequency. Use a large capacitor for C_e - this capacitor bypasses R_e for AC so that there is no AC negative feedback. Looking back into the emitter of the resistor, C_e sees $R_e \parallel [(r_{\pi}$ and base circuit resistors) / $\beta] \approx 8\Omega$.

For 8Ω with a 100Hz cutoff, $X_c = 1 / [2\pi f C_e] = 8\Omega$. Solve for $C_e = 1 / [2\pi * f * 8]$. Standard values are 10, 47, 100, and 220 μF .

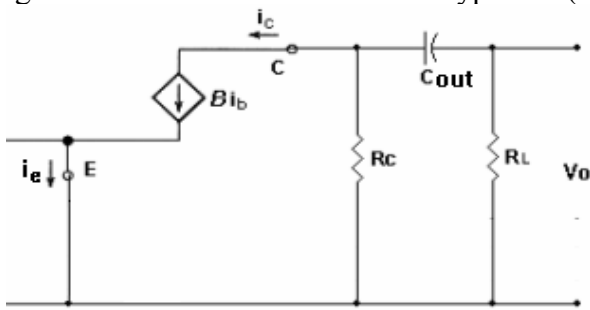
C_{in} The input circuit determines C_{in} . The output circuit is isolated from the input and can be ignored for this calculation and R_e is bypassed (shorted) by C_e . If you look at the model for the input part of the circuit, it looks similar to the Lab 4 highpass circuit. $f_{low} = 1 / 2\pi C_{in}(R_b \parallel r_{\pi} + R_{in})$



Arranging the cutoff equation from Lab 4 (with $R_b = R_1 \parallel R_2$) produces

$C_{in} = 1 / 2\pi f (R_b \parallel r_{\pi} + R_{in})$ Standard values are 0.1 μF , 1.0 μF , 4.7 μF , and 10 μF

C_{out} The output circuit determines C_{out} . The input circuit is isolated from the output and can be ignored for this calculation. R_e is bypassed (shorted) by C_e .

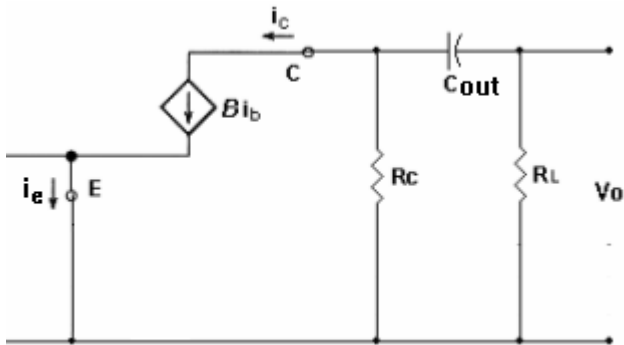


If you look at the model for the output part of the circuit, after a Norton to Thevenin transformation it looks similar to the Lab 4 highpass circuit. $f_{low} = 1 / 2\pi C_{in}(R_c + R_L)$

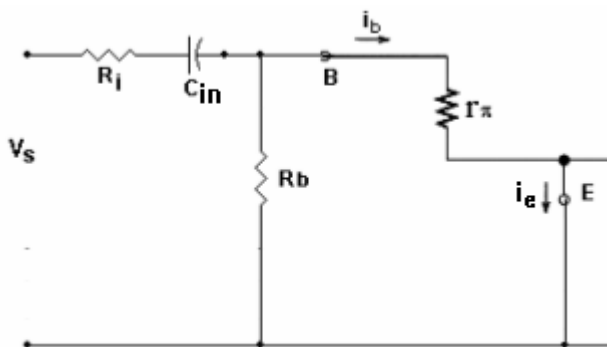
$C_{out} = 1 / 2\pi f (R_c + R_L)$ Standard values are 0.1 μF , 1.0 μF , and 4.7 μF

Passband Gain

To calculate the passband gain, consider the frequency to be high enough to short the capacitors. Note that the gain is negative because of the direction of the current source. Also note: dB is only calculated using the magnitude of the gain, so the “-”, which is a 180° phase shift, is ignored.



With C_{out} shorted, $V_o = -\beta i_b (R_L || R_c)$



With C_{in} shorted, $i_b = V_b / r_\pi$

by voltage division $V_b = V_s (r_\pi || R_b) / [(r_\pi || R_b) + R_{in}]$

If $r_\pi \approx 260\Omega$ and $R_b = R_1 || R_2 = 1800\Omega$, we can simplify $r_\pi || R_b$ to be $\approx r_\pi$

So $V_b \approx V_s r_\pi / (r_\pi + R_{in})$ and

$i_b = V_b / r_\pi \approx V_s r_\pi / r_\pi (r_\pi + R_{in}) = V_s / (r_\pi + R_{in})$

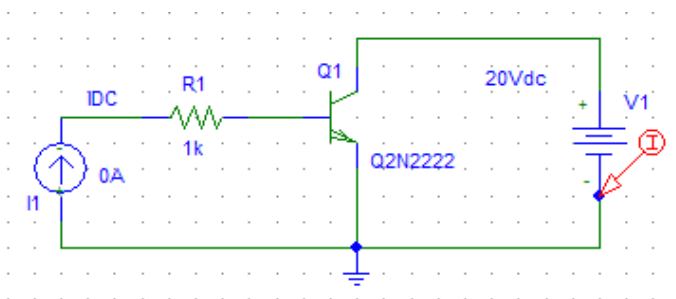
Now $V_o \approx -\beta V_s (R_L || R_c) / (r_\pi + R_{in})$

Passband Gain = $V_o / V_s \approx -\beta (R_L || R_c) / (r_\pi + R_{in})$

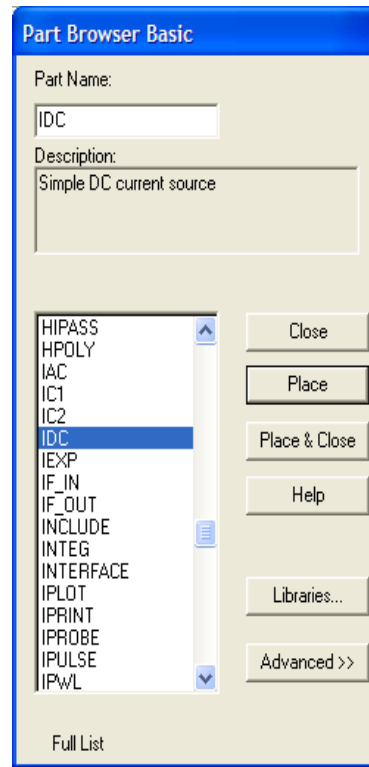
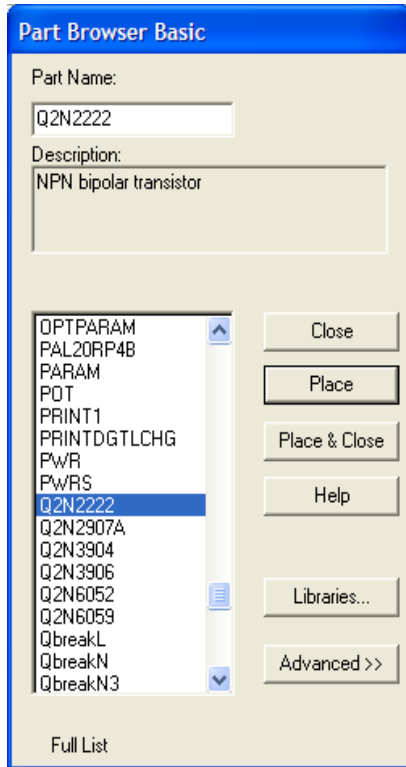
Passband Gain dB = $20 \log |V_o/V_s|$

Pspice simulations

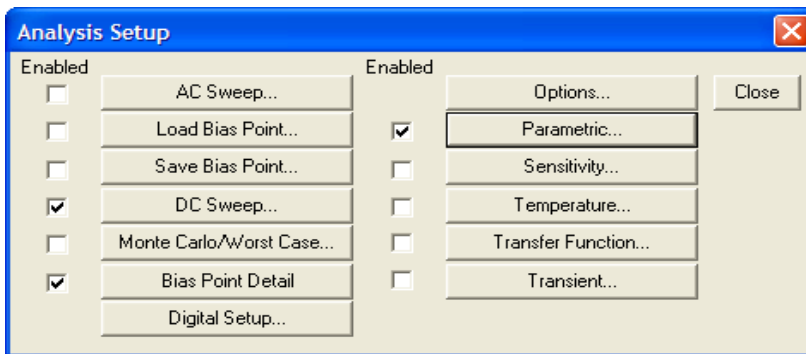
For the Curve trace generator, use this schematic:



The voltage source is VDC. Place VDC in the schematic and set it to 16 or 20V. The transistor is part Q2N2222. The current source is part IDC. Place IDC in the schematic and set the value to 0A.

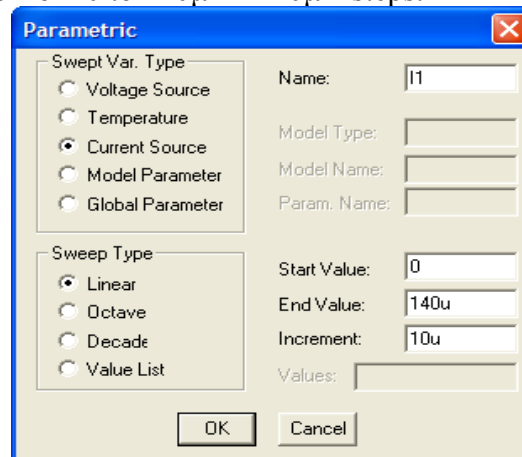
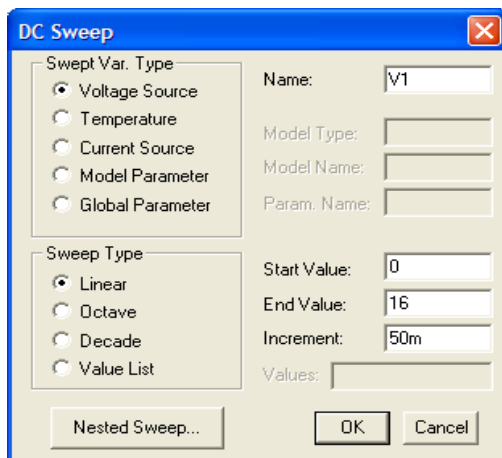


In the Analysis setup, enable DC Sweep, Bias Point Detail, and Parametric



Set the DC Sweep to run from 0V to 16V in 50mV steps.

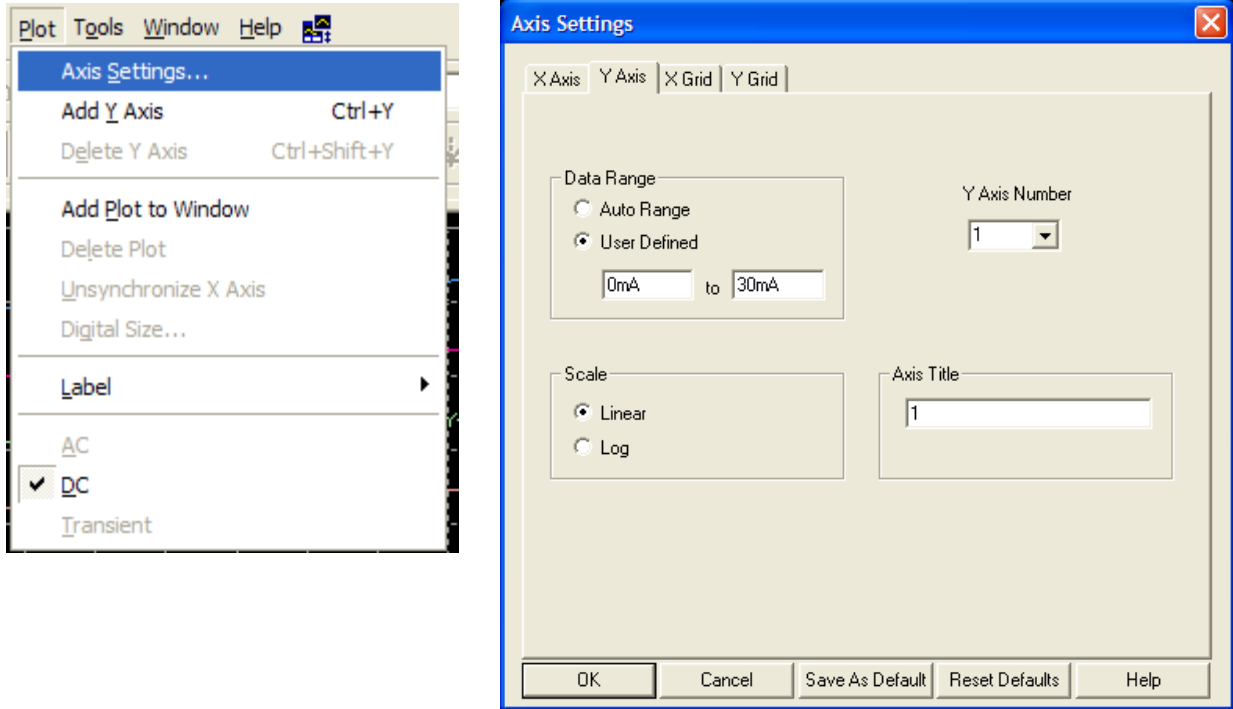
Set the Parametric sweep to step the current source from 0 to 140 μ A in 10 μ A steps.



Place a current probe to measure the current leaving the bottom of the DC supply. This will measure I_c .

Run the simulation. The results should be similar to the trace in Prelab question 1.

In the simulation, click Plot > Axis Settings > Y Axis > Select User Defined and set values 0A to 30mA.



Leave the X Axis set to Auto Range.

The display should then have 30mA for the top of the Y Axis and 16V for the end of the X axis.

For the Amplifier simulations

The clipping diodes are part number D1N4148.