ECE 3254
Digital Logic I
Laboratory #11
PRELAB

Name:
Partners:

Bench:

1. Read over the entire Lab 11 and the Prelab notes.

2. Complete the Logic Table for a 2-input NAND gate. Enter the expected output in Table 2, Part I- 2 on the Data Sheet.

Input A	Input B	Output Y
0	0	
0	1	
1	0	
1	1	

3. Design a 2-input AND gate using only 2-input NAND gates and complete the Logic Table. (Two NAND gates are required for this circuit)

↓ AND Circuit Design ↓

AND Logic Table

Input A	Input B	Output Y
0	0	
0	1	
1	0	
1	1	

Copy your circuit to Part III-1 on Page 6 of the lab and and the expected output to Table 4, Part III-1 on the Data Sheet.

4. Complete the Logic Table for a 3-input NAND gate. Enter the expected output in Table 5, Part III-2 on the Data Sheet.

Input A	Input B	Input C	Output Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	1	0	
1	1	1	

5. Complete the Logic Table for a <u>2-input</u> OR gate. Enter the expected output in Table 6, Part III-3 on the Data Sheet.

Input A	Input B	Output Y
0	0	
0	1	
1	0	
1	1	

6. Design a <u>2-input</u> NOR gate using only <u>2-input</u> NAND gates and complete the Logic Table. Hint: 4 gates are required; use DeMorgan's theorem. Copy your circuit to Part III-4 on page 7 of the Lab and enter the expected output in Table 7, Part III-4 on the Data Sheet.

↓ NOR Circuit Design ↓

NOR Logic Table

Input A	Input B	Output Y
0	0	
0	1	
1	0	
1	1	

7. When is it OK to connect logic gate inputs together?

8. When is it OK to connect logic gate outputs together?

9. What logic state will an unconnected gate input have?

10. If you have a four input logic gate and you are only using three of the inputs, what should you do with the unused logic input?

ECE 3254 **Name:**
Digital Logic I **Partners:**
Laboratory #11
Last Revised: 04-03-2009 **Bench:**

OBJECTIVES:

This lab introduces the basics of digital logic gates.

EXERCISES:

Part I : The Basic Inverter (NOT) and NAND Gates;
Part II : Valid Logic Level voltages
Part III : Combining Gates

It is very important that you recheck your wiring before turning on the power supply to avoid chip damage.

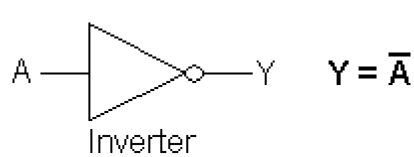
DO NOT leave any inputs open *on the gates that you are using*!!!! Unconnected inputs are not a logic low; they are not predictable and usually (but not always) float to the high input state. Inputs should always be connected to a gate output, a Logic High (+5V), or a Logic Low (0V or Ground).

NEVER connect logic outputs together (in parallel) to combine gates. If one gate says high output and the other says low output, the combined output can not be predicted and one or more of the conflicting chips may fail. Logic gate outputs have a specified current that they can produce. Logic inputs may be connected together (in parallel) as long as they do not overload the gate driving them.

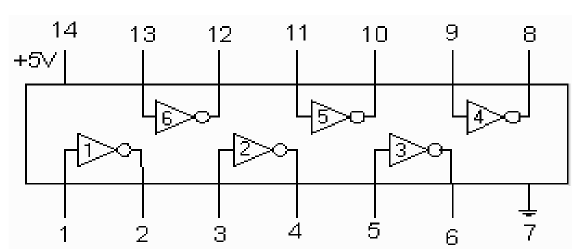
PART I: INTRODUCTION TO 7400 and 7404 LOGIC GATES

1. **The 7404 Inverter Gate (NOT =** The output is the invert of the logic input)
   Using your breadboard and DC supply, set the DC level to 5 volts and attach V_{CC} and ground to your 7404 chip. Logic inputs are pins 1, 3, 5, 9, 11, 13. Logic outputs are pins 2, 4, 6, 8, 10, 12.

   Measure the **actual output voltage levels** for any two of the gates. Use a jumper from the gate input pin (i.e. Pin 1 for the first gate) to pin 7 (ground) for a logic low, and then connect the jumper from the gate input pin to pin 14 for a logic high (+5V). **Note: An unconnected input is NOT A LOGIC LOW**, it is floating and its input state can not be predicted! Record your measurements in Table 1 on the Data Sheet.



Inverter logic symbol



The simplest logic chip is the 7404 hex inverter

2. **The 7400 NAND Gate** (contraction for NOT AND) is represented below.

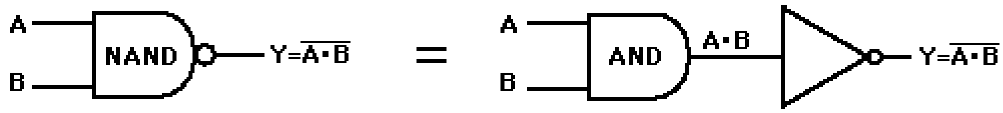


Figure 11-3 NAND Gate Representation

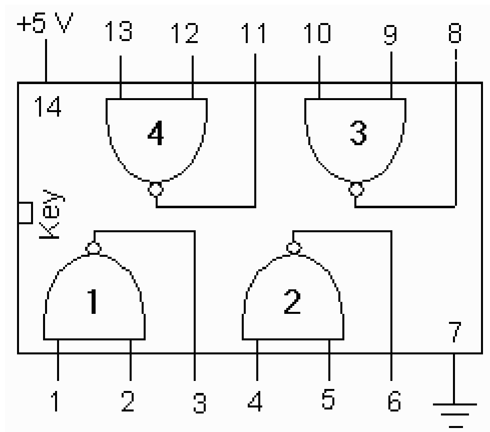
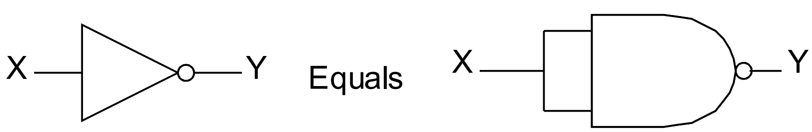


Figure 11-4 7400 Quad-2 Input NAND chip pin configuration.

Using your breadboard and DC supply set the DC level to 5 volts and attach VCC and ground to your 7400 chip. Verify the voltage and logic table for each of 4 NAND gates on the chip. Measure and record the **actual output voltage levels** and the observed output logic levels for all four gates in Table 2 on the Data Sheet.

Note: you will need all four gates on your 74LS00 chip for this lab. If your chip does not operate correctly, obtain a replacement and test it before you proceed.

3. **Inverter Gate (NOT) built with a <u>2 input</u> NAND Gate**



If the input gates of a NAND are connected together, there are only two input states: both inputs are high or both inputs are low. In part 2, you saw that the NAND output is1 if both inputs are 0; the output is 0 if both inputs are 1. Construct an inverter circuit using one 7400 NAND gate verify that the logic/voltage table matches the inverter from part I. **Note:** the actual voltage levels may differ slightly, but the logic states should be the same. Measure and record the actual output voltage levels and the observed output logic levels in Table 3 on the Data Sheet.

PART II: MEASUREMENT TO DETERMINE VALID LOGIC LEVELS

Logic Low (0) input: A logic low output is typically defined as 0V, but many chips are not able to produce a 0V output. There is actually an input voltage range (typically 0V to 0.5V) that produces a logic low output in a driver gate (or a logic high output in an inverter gate).

Logic High (1) input: A logic high output is usually defined as 5V, but few chips are actually able to produce a 5V output. The "high" input range, typically from 1.5V to 5V, produces logic high in a driver (or a logic low in an inverter).

Invalid logic inputs: A gate connected to a voltage between the logic low range and the logic high range (approximately 0.5V to 1.5) will not have a predictable output state, and the gate output may toggle between logic low and high states. Additionally, to prevent chip damage, 7400 series logic gate inputs must never be connected to voltages below 0V or above the supply voltage of +5V.

1. Wire the NAND gate inverter in Figure 11-1.
   Attach the +VCC (pin 14) to the constant +5V power supply.
   Connect the swept power supply to the NAND gate inputs (pins 1 and 2).
   Connect the multimeter to the NAND gate output (pin 3).

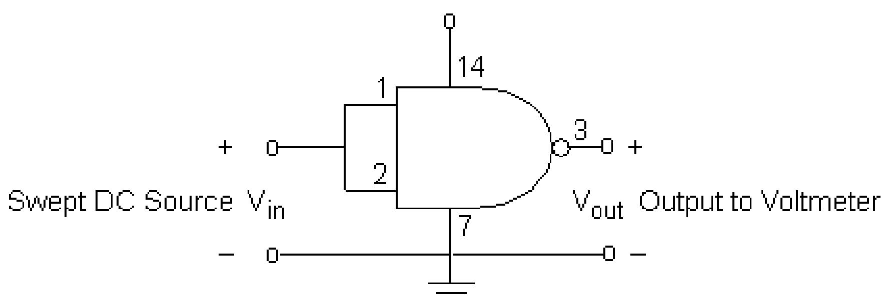


Figure 11- 1 Threshold Measurement Circuit

   NOTE: You must use two power supplies - one constant +5V supply to power the chip, and another supply for the input voltage sweep. It is easier to set the Agilent supply to power the chip and sweep the Phillips supply.

2. Set up Lab Workbench's DC Sweep for an input voltage range of 0 to 5 volts in steps of 0.1 volts (51 steps) and perform the sweep.

   NOTE: Use the Labview menu to verify that the the meter will be set to measure DC volts.

3. Using the buffer to examine the DC sweep results, determine the approximate V_L (the input voltage where the gate output voltage begins to drop from the high state) and V_H (the input voltage where the output voltage has dropped completely to the low state). **Remember that this circuit is an inverter**, so a low input produces a high output and a high input produces a low output. **You are measuring the input logic levels.** Record your measured input VH and VL on the data sheet, and determine the input voltages corresponding to valid logic levels, and invalid input voltage levels.

   Valid logic input levels: An input logic state 0 (low) corresponds to any voltage level between 0V and the break voltage V_L. An input logic state 1 (high) corresponds to any voltage level between the break voltage V_H and 5V.
   Invalid logic input levels: To prevent false logic triggering, a voltage between V_L and V_H is

considered to be an invalid logic signal. To prevent damage to a logic gate, the input voltage should never be less than 0V or greater than the +5V supply voltage.

Save the sweep as a jpeg file. Position the red cursor to indicate input V_L and the blue cursor to indicate input V_H. Record V_H and V_L on the data sheet.

Print the jpeg and clearly label the axes, the threshold voltages (V_L and V_H), and the **ranges** corresponding to a logic low input, a logic high input, and invalid input voltages. Write all names on the print, title the print and attach the print to one of the lab reports.

PART III: COMBINING LOGIC GATES

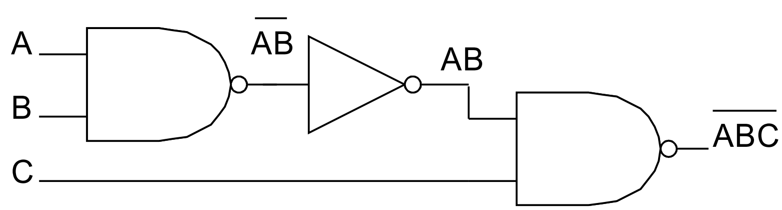
1. AND Gate Y=A+B built with <u>2 input</u> NAND gates

↓ AND circuit From Prelab ↓

Build the AND circuit you designed in the prelab, test the circuit, and complete the truth table. Use a NAND gate to build the inverter required for this circuit.

2. <u>3 input</u> NAND Gate $Y=\overline{A \bullet B \bullet C}$ built with <u>2 input</u> NAND gates

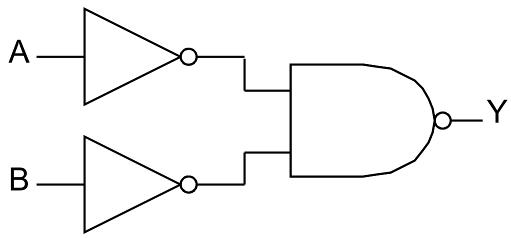
A <u>3 input</u> NAND (the 7410 contains three) is easily constructed using a combination of <u>2 input</u> NAND gates. Construct the following circuit with your 7400 chip and verify the <u>3 input</u> NAND function. Use one of the NAND gates on the 7400 to build the inverter required for this circuit.



Measure the output voltages and logic levels for all possible input states and record the results in Table 5 on the Data Sheet.

3. OR gate Y=A+B built with NAND Gates

Construct and verify an OR gate from a NAND and two inverters. Use NAND gates to build the inverters required for this circuit.



Measure the output voltage for all possible input states and record the results in Table 6 on the Data Sheet.

4. NOR Gate $Y=\overline{A+B}$ built with NAND Gates

↓ **NOR Circuit Design (from Prelab)** ↓ Construct and verify the NOR gate you designed.

Measure the output voltage for all possible input states and record the results in Table 7 on the Data Sheet.

5. (5 points) Shut down Windows, return cables to racks, return parts to correct drawer bins, return adapters to container, turn off power, clear bench, and place seat under bench.

ECE 3254 Lab 11 Data Sheet

Name_____________________ **Date**______________

Partner ________________ **Bench**_________

PART I: INTRODUCTION TO 7400 and 7404 LOGIC GATES

1. Table 1 – Inverter Measurements

Input		Observed Output			
Voltage	Logic Level	Y1 Voltage	Y1 Logic Level	Y2 Voltage	Y2 Logic Level
0V	0				
+5V	1				

2. Table 2 – NAND Gate Measurements

Input V		Measured Output Voltage				Logic Level						
						Expected			Observed			
A	B	Y1	Y2	Y3	Y4	A	B	Y	Y1	Y2	Y3	Y4
0	0					0	0					
0	+5					0	1					
+5	0					1	0					
+5	+5					1	1					

3. Table 3 – NAND Gate Inverter Measurements

7404 Inverter – **Use values from I-1**

Voltage		Logic Level	
X	Y	X	Y
0			
+5			

7400 NAND Connected as Inverter

Voltage		Logic Level	
X	Y	X	Y
0			
+5			

Compare the NAND inverter logic and voltage levels with the Inverter of Part II-1.

PART II: MEASUREMENT TO DETERMINE VALID LOGIC LEVELS

3. **Measured:** Input V_H = ____________ Input V_L = ______________

A digital input 0 is represented by voltages between ________ and ________.

A digital input 1 is represented by voltages between ________ and ________.

Invalid logic input voltage ranges are:

PART III: COMBINING LOGIC GATES

1. **Table 4 - AND Gate**

Voltage			Y Logic Level	
A	B	Y	Observed	Expected
0	0			
0	+5			
+5	0			
+5	+5			

How do your voltage and logic level measurements compare to the expected results for the AND gate?

2. **Table 5 - <u>3 input</u> NAND Gate**

Voltage				Y Logic Level	
A	B	C	Y	Observed	Expected
0	0	0			
0	0	+5			
0	+5	0			
0	+5	+5			
+5	0	0			
+5	0	+5			
+5	+5	0			
+5	+5	+5			

How do your voltage and logic level measurements compare to the expected output for a 3 input NAND gate?

3. **Table 6 - OR gate**

Voltage			Y Logic Level	
A	B	Y	Observed	Expected
0	0			
0	+5			
+5	0			
+5	+5			

How do your voltage and logic level measurements compare to the expected output for a OR gate?

4. **Table 7 - NOR gate**

Voltage			Y Logic Level	
A	B	Y	Observed	Expected
0	0			
0	+5			
+5	0			
+5	+5			

How do your voltage and logic level measurements compare to the expected output for a NOR gate?