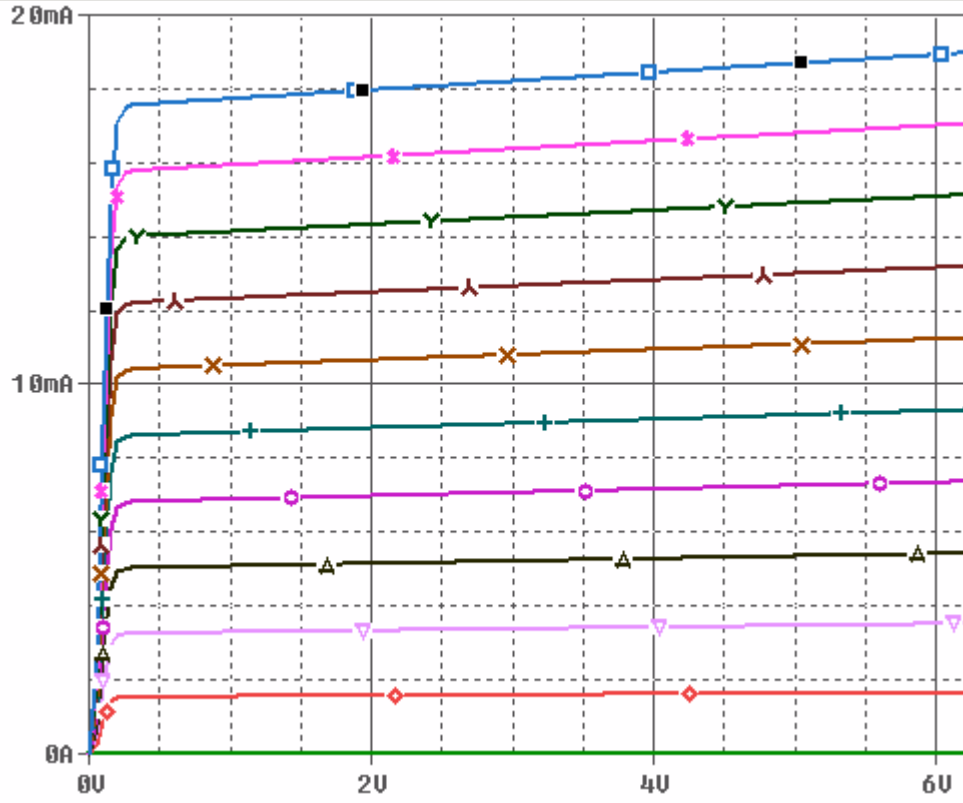


Read over the entire Lab 7. Show all work (equations, values, etc) for credit.

1. On the curve trace below, label the three operating regions of a transistor. (3 points)



Describe the characteristics of each region (think in terms of the relationships between  $I_C$ ,  $I_B$ ,  $\beta$ ,  $V_{CE}$  &  $V_{BE}$ ). (5 points)

2. For the bias circuit in Fig 7-2, choose values for  $V_E$ , and  $V_C$ . Calculate  $V_B$ ,  $V_{CE}$ ,  $V_{BE}$ , and  $I_B$  ( Show reasons for values of  $V_E$ ,  $V_C$ ,  $V_{CE}$ ,  $V_{BE}$ ) Write these values in Part II-1 of the Data Sheet. (5 points)

$V_E =$  \_\_\_\_\_,  $V_C =$  \_\_\_\_\_,  $V_B =$  \_\_\_\_\_,  $V_{CE} =$  \_\_\_\_\_,  $V_{BE} =$  \_\_\_\_\_,  $I_B =$  \_\_\_\_\_

3. Using your  $V_C$  and  $V_E$  for the bias circuit in Fig 7-2, calculate the values for  $R_e$ ,  $R_c$ ,  $R_1$ , and  $R_2$ . Write your values on fig 7-2 for reference in the lab. **(12 points)**

$R_e =$  \_\_\_\_\_,  $R_c =$  \_\_\_\_\_,  $R_1 =$  \_\_\_\_\_,  $R_2 =$  \_\_\_\_\_

4. Apply the small signal model to the amplifier circuit in Figure 7-3 and calculate  $r_\pi$ . Solve for the **passband voltage gain**,  $A_v = V_L/V_s$ . Assume that the DC source  $V_{CC}$  is bypassed to ground for AC signals. Enter the results below and on Part III-1 of the Data Sheet. **(8 points)**

$r_\pi \approx$  \_\_\_\_\_,  $A_v = V_o / V_s =$  \_\_\_\_\_ = \_\_\_\_\_ dB in the passband.

5. Use the AC small signal model to solve for a  $C_e$  value so that the cutoff frequency determined by  $C_e$  is 100 Hz. Enter the results below and on Part III-2 of the Data Sheet. Hint: the input circuit is very similar to Lab 3. **(4 points)**

$C_e =$  \_\_\_\_\_ Write this value on Fig 7-3 for reference in the lab.

6. Use the AC small signal model to solve for a value for  $C_{in}$  so that the cutoff frequency determined by  $C_{in}$  is 100 Hz. Enter the results below and on Part III-2 of the Data Sheet. Hint: the input circuit is very similar to Lab 3. **(4 points)**

$C_{in} =$  \_\_\_\_\_ Write this value on Fig 7-3 for reference in the lab.

7. Use the AC small signal model to solve for a value for  $C_{out}$  so that the cutoff frequency determined by  $C_{out}$  is 100 Hz. Enter the results below and on Part III-2 of the Data Sheet. Hint: the input circuit is very similar to Lab 3. **(4 points)**

$C_{out} =$  \_\_\_\_\_ Write this value on Fig 7-3 for reference in the lab.

8. Use Pspice to generate a curve trace for the 2N2222 transistor. **(8 points)**  
Display for  $0 < V_{CE} < 16V$  and  $0 < I_C < 30mA$ . Step the base current 14 times in  $10\mu A$  steps.  
In the top right corner, use the Label tool to add your name and ECE3254 Lab 7 Curve Trace to the simulation results.

Print the simulation and hand label the value for each  $I_B$  trace (values range from 0 to  $140\mu A$ ) on the right hand of the print Draw the load line for the resistor values you calculated in question 3 and indicate on the load line the Q point for  $I_C$  and  $V_{CE}$  where your transistor will be operating. Note:  $I_B$  from the prelab calculation does not hit the Q point because the  $\beta$  used by Pspice is higher than 150. Attach the print to the Prelab.

9. Build the Bias circuit of Fig 7-2 in Pspice. Set the components to the values you calculated and turn on the V and I bias displays. Run the simulation to display the circuit's voltages and currents. If the values are not similar to the expected values from your Prelab design, check your Prelab calculations and Pspice component values. **(7 points)**

$V_C =$  \_\_\_\_\_,  $V_E =$  \_\_\_\_\_,  $V_B =$  \_\_\_\_\_

$I_C =$  \_\_\_\_\_,  $I_B =$  \_\_\_\_\_

Calculate:  $V_{CE} =$  \_\_\_\_\_,  $V_{BE} =$  \_\_\_\_\_

Record these bias values in Part II-1 on the Data Sheet.

On the schematic information box at the bottom, enter at least your name, ECE 3254 Lab 7 CE Amplifier Bias, and the date. Print the Schematic with the Bias values showing. **(5 points)**

10. Enter the rest of the Amplifier circuit of Figure 7-3 into Pspice. On the schematic information box at the bottom, enter at least your name, ECE 3254 Lab 7 CE Amplifier, and the date. **(14 points)**

With the bias display turned off, Run a transient simulation from  $t=0$  to  $t=3\text{ms}$  with **0.05ms steps** to capture  $V_S$  and  $V_L$ . On the simulation, use the cursor to measure and label the values for  $V_{Smin}$ ,  $V_{Smax}$ ,  $V_{Lmin}$  and  $V_{Lmax}$ . Use the Label tool to place your name and ECE3254 Lab 7 Amplifier Transient Response on the simulation. Print the schematic and simulation, and attach them to the Prelab. **(14 points)**

$$V_{Smin} = \underline{\hspace{2cm}}, V_{Lmin} = \underline{\hspace{2cm}}$$

$$V_{Smax} = \underline{\hspace{2cm}}, V_{Lmax} = \underline{\hspace{2cm}}$$

$$AV = -V_{Lpp}/V_{Spp} = \underline{\hspace{2cm}} = \underline{\hspace{2cm}} \text{ dB}$$

Record the values for AV in Part 3-1 of the Data Sheet.

How does AV compare to the Prelab calculation? **(3 points)**

11. Use Pspice to obtain a frequency response for the Amplifier circuit for 10Hz to 10kHz. Use the AC decade sweep with at least 50 points per decade. Add a trace for dB gain. Use the cursor to find and label  $V_{Smax}$ ,  $V_{Lmax}$  and dBmax (in the passband). Use the cursor to find and label the cutoff frequency. **(12 points)**

$$V_{Smax} = \underline{\hspace{2cm}}, V_{Lmax} = \underline{\hspace{2cm}}, \text{dBmax} = \underline{\hspace{2cm}}, f_{low} = \underline{\hspace{2cm}}$$

Record dBmax and  $f_{low}$  in Part 3-2 of the Data Sheet.

How do dB max and  $f_{low}$  compare to the expected values? **(4 points)**

## ECE 3254

### Analysis of an NPN Transistor Amplifier

#### Laboratory #7

Last Revised: 10-08-2009

#### OBJECTIVES:

The bipolar junction transistor is a current amplifier with  $I_C = \beta I_B$ . You will examine BJT voltage gain, the characteristics of BJT active and saturation regions of operation, simple BJT DC biasing, and BJT AC (amplifier) design and analysis.

#### EXERCISES:

This laboratory is broken into three parts:

- PART I: BJT DC Analysis
- PART II: BJT DC Bias Design
- PART III: BJT AC Analysis

#### PART I: BJT DC ANALYSIS

1. This step deleted – you will not use the curve tracer. The load line will be placed on the curve trace from Pspice that follows the Data Sheet.
  
2. Construct the circuit given in Figure 6-1. For  $R_B$ , use a 47k resistor in series with the decade box. Use 100 $\Omega$  for  $R_e$  and 470 $\Omega$  for  $R_c$ .

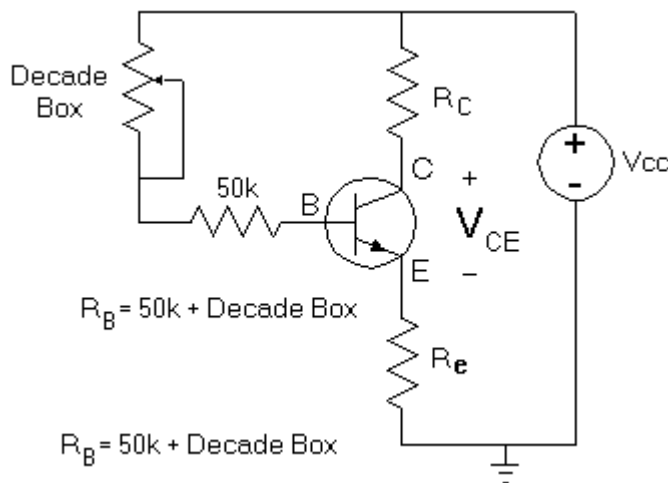


Figure 7-1 BJT Biasing Circuit

3. After setting  $V_{CC}=15V$ , begin with  $R_B$  set to 147 k $\Omega$  ( $R_B = 47k\Omega +$  Decade Box setting) and adjust  $R_B$  until  $V_E = 1.51V$  ( $I_C \approx 15ma$ ). **NOTE:** Use wires, clipped into the mini-grabber, to probe the transistor voltages. If you attempt to connect a mini-grabber directly to the transistor, you will probably short the base and blow the transistor.

Allow the transistor to warm up and stabilize (~10 seconds) - you may have to adjust  $R_B$ . When  $V_E = 1.51V$ , record the value of  $R_B$ . Measure  $V_B$ ,  $V_E$  and  $V_C$ , then calculate  $V_{BE}$ ,  $V_{CE}$ ,  $V_{RB}$ ,  $V_{RC}$ ,  $I_B$ ,  $I_C$ , and  $\beta = I_C/I_B$ . Record the Q point (bias operating point of  $I_C$ ,  $I_B$ , &  $V_{CE}$ ) values on the data sheet.

- Adjust  $R_B$  until the transistor saturates ( $V_{CE} < 0.2V$ ). Allow the transistor to warm up and stabilize. On the Data Sheet, record the measured & calculated Q point values.
- On the curve trace (from Pspice) that follows the Data Sheet, draw the load line, clearly indicate each of the load line end points, the *operating ranges* (active, saturated, and cutoff) and the two operating points measured in steps 3 and 4. NOTE: Everything should lie along a straight "load line", but  $I_B$  may not match if your transistor  $\beta$  differs from the Pspice model.

## PART II: BJT Common Emitter Amplifier Bias Measurements

- Build amplifier bias circuit in fig 7-2 using the values you Prelab values you chose for the amplifier.

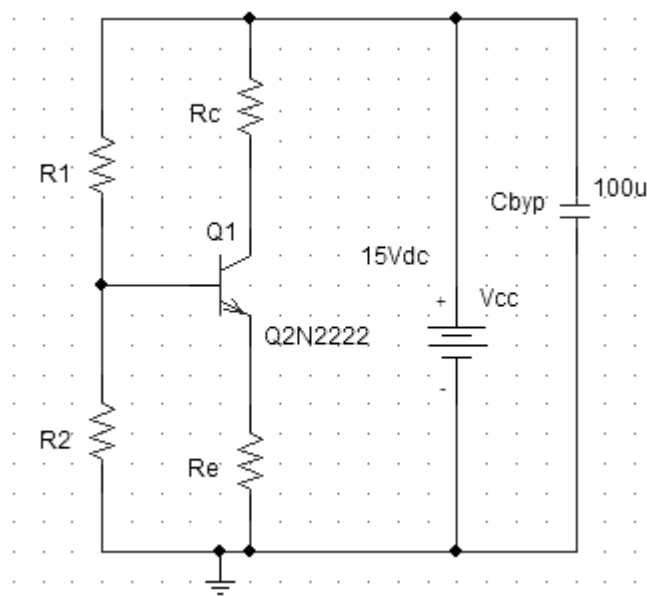
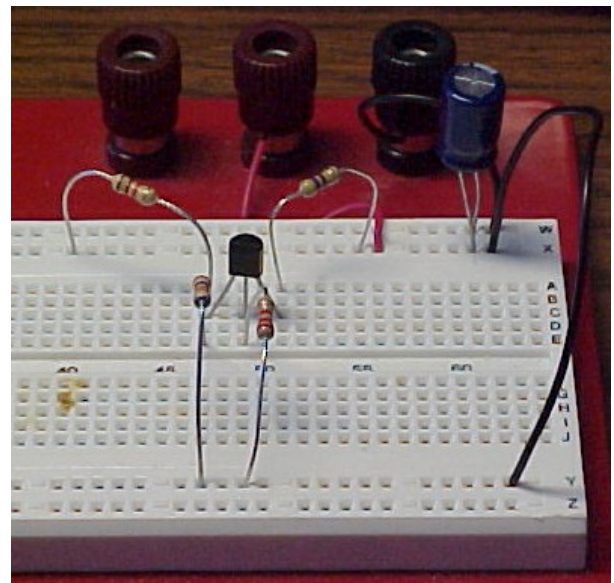


Figure 7-2 CE Amplifier Bias Circuit



Suggested Circuit Layout

Measure  $V_C$ ,  $V_E$ ,  $V_B$ , and calculate  $V_{CE}$ ,  $V_{BE}$ ,  $I_C$ , and  $I_B$ . On the Data Sheet, compare your results to the calculated and simulated values from the Prelab and Pspice. If the values are not similar, troubleshoot the circuit.

$$V_{CE} = V_C - V_E$$

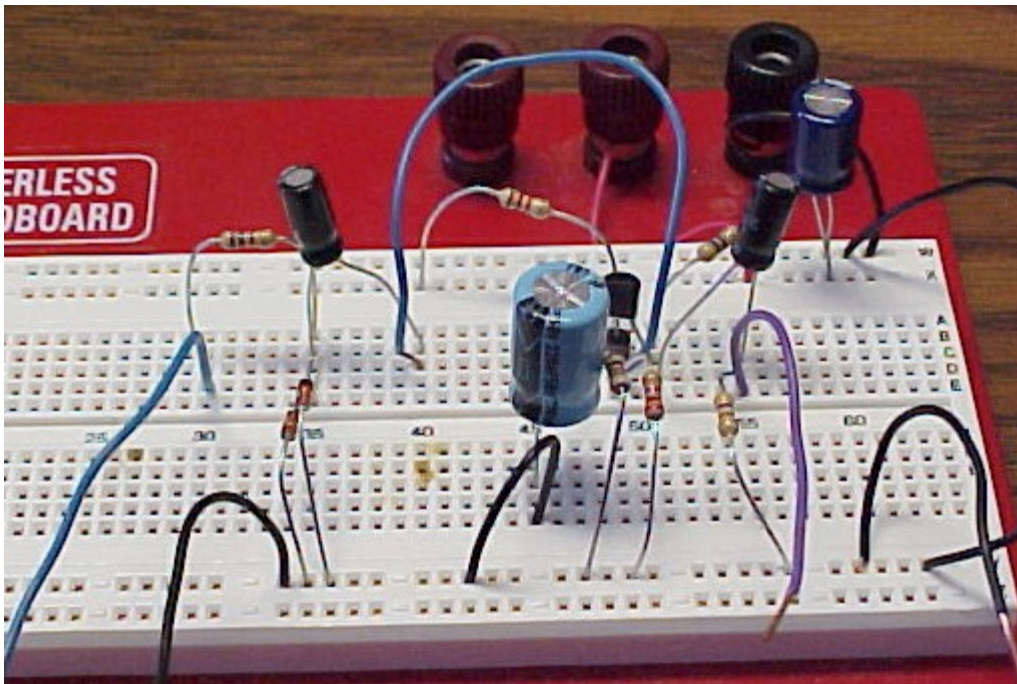
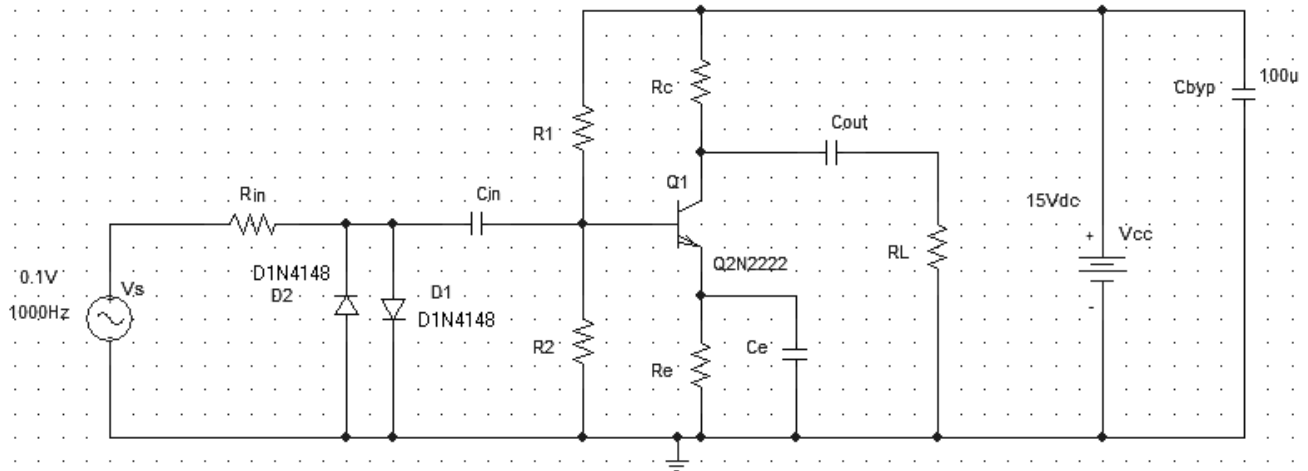
$$V_{BE} = V_B - V_E$$

$$I_C = (V_{CC} - V_C) / R_C$$

$$I_B = I_{R1} - I_{R2} = [ (V_{CC} - V_B) / R1 ] - [ V_B / R2 ]$$

### PART III: BJT AC ANALYSIS

1. Add components to the bias circuit to complete the amplifier circuit in Fig 7-2. Use the component values that you used in the Pspice simulation.



Suggested Layout

Set  $R_{in} = 1000\Omega$  and  $R_L = 2200\Omega$ . Use the function generator to input a 1000 Hz,  $0.2V_{pp}$  AC signal into the amplifier. Use the oscilloscope to measure  $V_o$  with CH1 (make sure that  $V_o$  is an undistorted sine wave), and measure  $V_s$  with CH2. **NOTE:** Use wires, clipped into the mini-grabber, to probe the voltages. Calculate the voltage gain  $V_L/V_s$ . Record your results on the data sheet.

Capture the Scope waveforms and print them. Position the cursors to measure  $V_{S_{max}}$  and  $V_{L_{max}}$ . On the Data Sheet, compare your captures to the Pspice simulation (amplitudes, waveform shape, etc).

2. Use the computer to make an AC sweep measurement of the amplifier's frequency response from 10Hz to 10kHz with 75 data points and a  $0.2V_{pp}$  sinusoidal input signal.

Save the AC sweep response as a jpeg file. Normalize the response to Vs. Use the red cursor to indicate  $\text{dB}_{\text{max}}$  (maximum passband output response) and the blue cursor to indicate the cutoff frequency  $f_{\text{low}}$  (3 dB down from max). Record the measured passband gain and the cutoff frequency on the Data Sheet.

**Print the frequency response jpeg.** Title your print, label the cutoff frequency, passband, and  $\text{dB}_{\text{max}}$ , write your name on the print, and attach the print to your Data Sheet.

3. Shut down Windows, return cables to racks, return parts to correct drawer bins, return adapters to container, turn off bench power, clear bench, and place seat under bench. (5 points)

100 points total

Names: \_\_\_\_\_

by first name: 3<sup>rd</sup> alphabetically – wiring      1<sup>st</sup> alphabetically – Labview      2<sup>nd</sup> alphabetically– data sheet

**PART I: BJT DC Analysis**

3.  $R_B =$  \_\_\_\_\_  $V_B =$  \_\_\_\_\_  $V_E =$  \_\_\_\_\_  $V_C =$  \_\_\_\_\_

$V_{BE} =$  \_\_\_\_\_  $V_{CE} =$  \_\_\_\_\_

$V_{RB} = V_{CC} - V_B =$  \_\_\_\_\_  $I_B =$  \_\_\_\_\_

$V_{RC} = V_{CC} - V_C =$  \_\_\_\_\_  $I_C =$  \_\_\_\_\_  $\beta = I_C / I_B =$  \_\_\_\_\_

4.  $R_B =$  \_\_\_\_\_  $V_B =$  \_\_\_\_\_  $V_E =$  \_\_\_\_\_  $V_C =$  \_\_\_\_\_

$V_{BE} =$  \_\_\_\_\_  $V_{CE} =$  \_\_\_\_\_

$V_{RB} = V_{CC} - V_B =$  \_\_\_\_\_  $I_B =$  \_\_\_\_\_

$V_{RC} = V_{CC} - V_C =$  \_\_\_\_\_  $I_C =$  \_\_\_\_\_  $I_C / I_B =$  \_\_\_\_\_ ( $\neq \beta$ )

**PART II: BJT BIAS DESIGN (DC)**

1. Q-point measurements and circuit component values.

	<i>From Prelab</i>	<i>From Pspice</i>	<b>Measured/Calculated</b>
$V_C$	_____	_____	_____
$V_E$	_____	_____	_____
$V_B$	_____	_____	_____
$V_{CE}$	_____	_____	_____
$V_{BE}$	_____	_____	_____
$I_C$	<b>15mA</b>	_____	_____
$I_B$	_____	_____	_____

How do your measured bias points compare to the measurements for  $V_{CE}$ ,  $V_{BE}$ ,  $I_C$  and  $I_B$  from Part I-3?

How do your measured bias points compare to the design values and Pspice simulation results for  $V_{CE}$ ,  $V_{BE}$ ,  $I_C$  and  $I_B$  ?

What is responsible for the differences between the measured values and the expected values?

### PART III: BJT AC ANALYSIS

1. From the Prelab calculation:  $V_o/V_s = \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$  dB (at 1000Hz)

From the Pspice simulation:  $V_o/V_s = \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$  dB (at 1000Hz)

Measured  $V_s = \underline{\hspace{2cm}} V_{pp}$   $V_o = \underline{\hspace{2cm}} V_{pp}$  Output phase =  $\underline{\hspace{2cm}}$

Measured  $V_o/V_s = \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$  dB (at 1000Hz)

How closely does the measured gain match the predicted gain? (NOTE: If you are not in the ballpark, troubleshoot your circuit.)

2. From the Prelab calculation: Gain =  $\underline{\hspace{2cm}}$  dB in the passband,  $f_{low} = 300\text{Hz}$

From the Pspice AC Sweep: Gain =  $\underline{\hspace{2cm}}$  dB in the passband,  $f_{low} = \underline{\hspace{2cm}}$

Measured passband gain =  $\underline{\hspace{2cm}}$  dB (normalized to  $V_s = 0.2V_{pp}$ )

Measured cutoff frequency  $f_{low} = \underline{\hspace{2cm}}$  Hz

How do the measured values of Gain and  $f_{low}$  compare to your calculations and Pspice simulation? Explain what might be responsible for differences.

