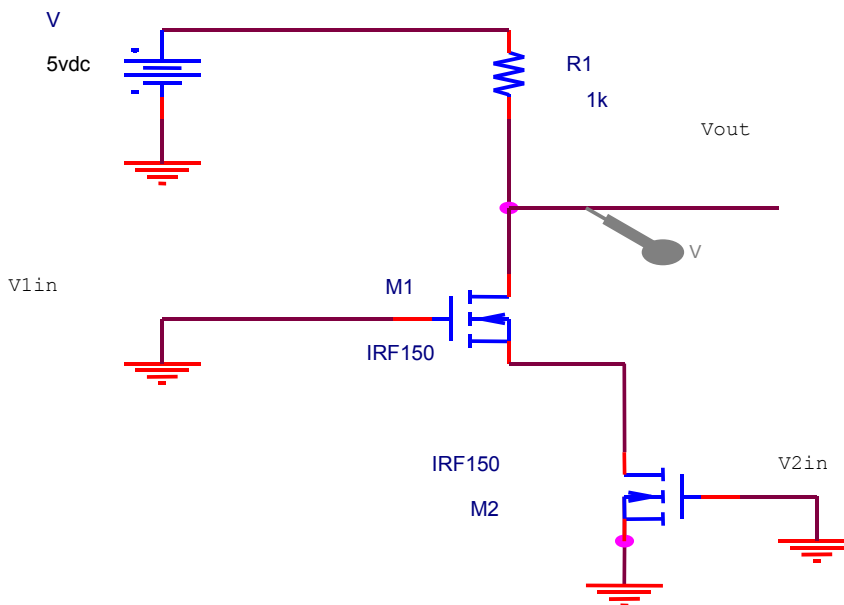


EE2274
Pre-Lab for Experiment 11
NAND Gate, NOR Gate, and S-R Latch

NMOS NAND Gate

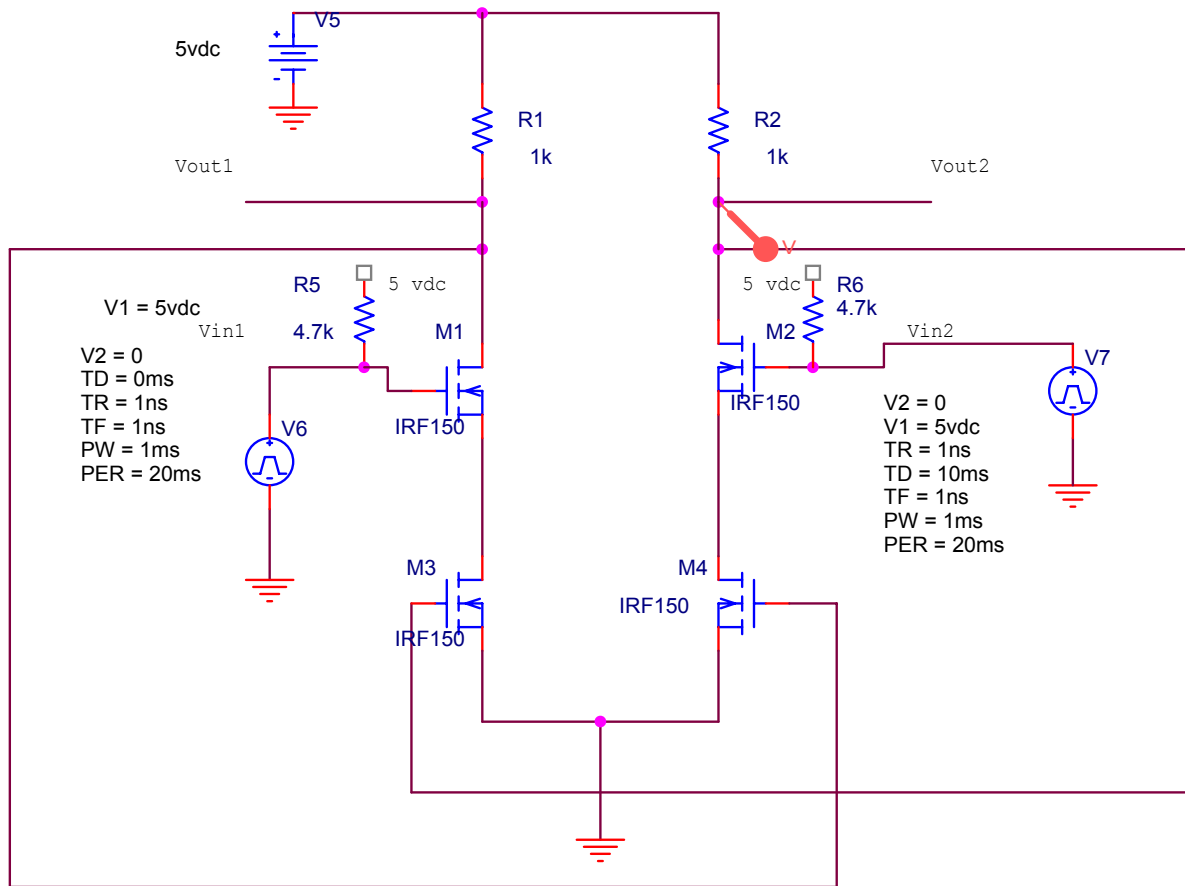
1. For the NMOS NAND gate shown below assume a 5 volt input as a logic “1” and ground as a logic “0”. Make a truth table showing the four possible combinations of Vin1 and Vin2 and the outputs Then run a DC Bias Point simulation on your design with the four possible input combinations for Vin1 and Vin2 to verify your gate. Observe the output voltage value for each input combination. Print your circuit schematic showing voltages for all four input combination.



NMOS NAND GATE

NMOS NOR Gate

2. Design an NMOS NOR gate using the IRF150. Show all work for your design. Then simulate your design in PSpice with DC Bias Point simulations as you did for the NAND gate. Print out your circuit schematic showing voltages for all four input combination. Also, fill in the truth table with all of the Bias Point simulation voltage values.



NMOS S-R Latch

N

MOS S-R Latch

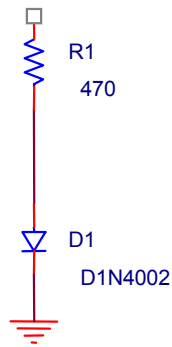
In PSpice, build an S-R Latch using NMOS NAND gates. To verify the operation of the S-R Latch set up the two pulsed inputs. The inputs will go from 5 vdc to ground to make the latch S-R Latch work. Verify the operation of your circuit by plotting and copying the waveforms.

PSpice hints for the S-R Latch.

Run s “Time Domain” for 100ms. Under “plot” use “add plot window” and add two additional windows. Then go to “add trace”and separate the waveforms with Vin1 into the top window Vin2 into the middle window and Vout into the bottom window. This will demonstrate how the S-R Latch works.

Laboratory Exercise
Experiment 11
NAND GATE, NOR GATE, and S-R LATCH

1. Build the NAND gate, but add a LED. Instead of measuring the output voltage levels, you will use the LED to verify the NAND gate's operation. Try all of the input combinations. Connect the circuit below to V_o . Use a LED instead of the diode.



2. Build the NOR gate that you designed in the Pre-Lab. Again, use an LED with current limiting resistor in series with it to determine the output states. Verify the truth table for a NOR gate.
3. Build the S-R Latch from the Pre-Lab. Add the LED circuit as you did for the NAND and NOR gate. Try the four input combinations on the S-R Latch. What happens when you use the indeterminate input combination of logic 1 on both inputs?

DATA SHEET
Experiment 11
NAND GATE, NOR GATE, and S-R LATCH

1. NAND GATE

Vin1	Vin2	LED (on or off)

2. NOR GATE

Vin1	Vin2	LED (on or off)

4. NMOS S-R Latch

Vin1	Vin2	Vout1 LED	Vout2 LED