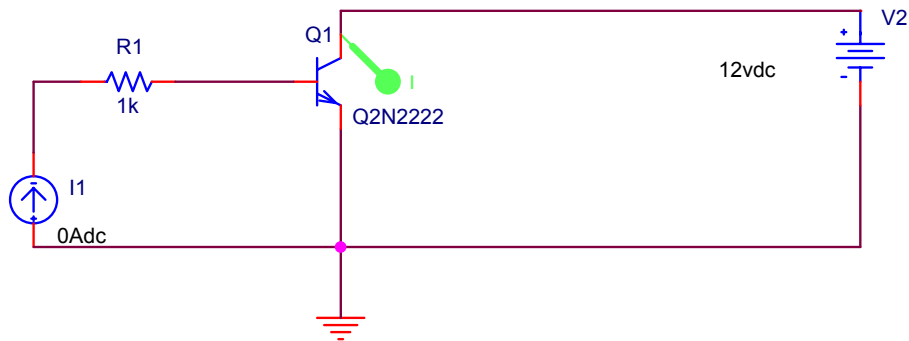


**EE 2274**  
**Pre-Lab for Experiment #10**  
***BJT Biasing***

**1. Common Emitter (CE) Output Characteristics**

**Generate the output characteristics curves for a 2N2222 in PSpice. Label your graph and determine the dc beta of the transistor from your graph. Show all work.**

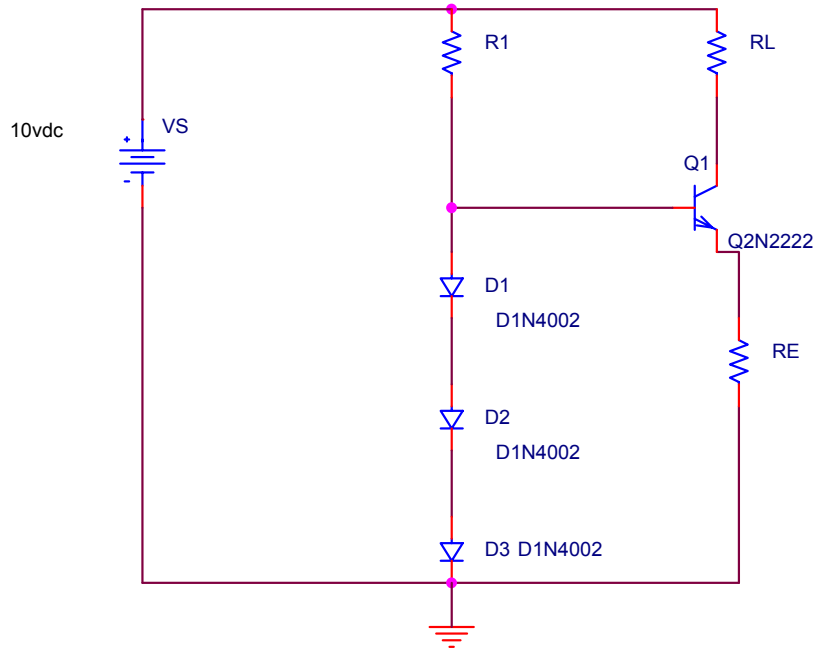
**Use the circuit below for your model. A couple of PSpice hints, use the Parametric and Primary Sweeps to generate your graph. Parametric Sweep Spec. 0 to 50ua in 5ua increments. Primary Sweep Spec. 0 to 12v in 200 mv increments.**



Common Emitter(CE)

### Diode Current Source

Shown below is a current source made from an NPN transistor. The three diodes bias the base of the transistor at 1.8V. Design for 1ma through RL. Assume current through R1 is 10 times  $I_B$ . Also, assume  $\beta = 100$ . Find maximum value for RL?



### NPN Diode Current Source

As long as the base to emitter is forward biased ( $V_B > V_E$  .6V to .7V) ensures the emitter of the transistor is always conducting.

The voltage and current of the emitter is as follows:

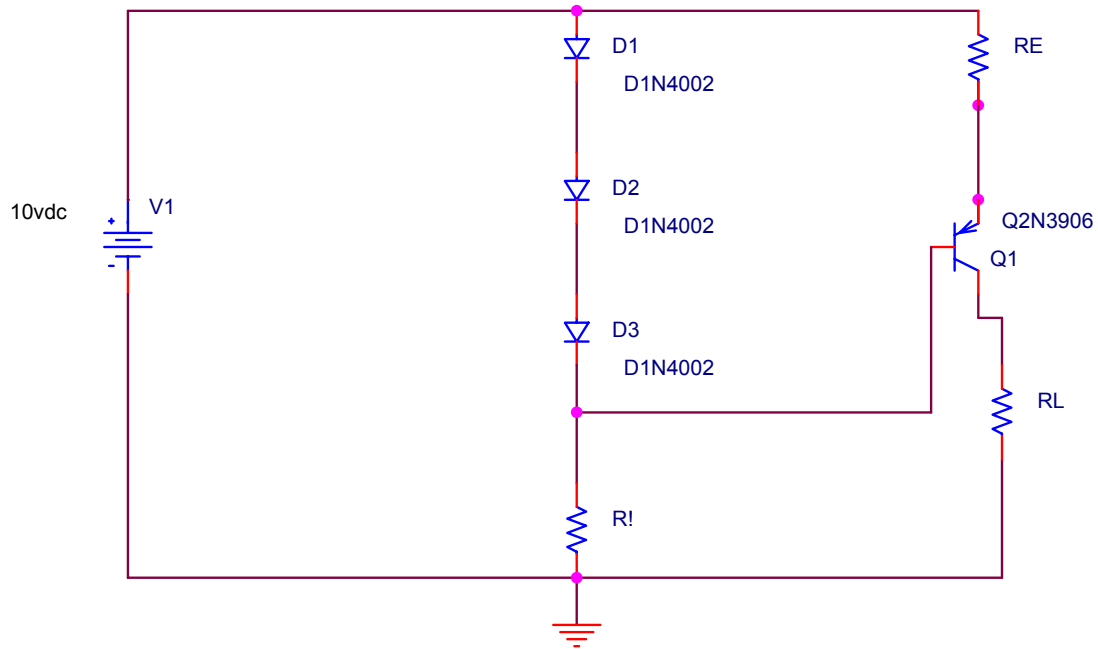
$$V_E = V_B - 0.6V, \text{ and thus } I_E = V_E/R_E = (V_B - 0.6V)/R_E.$$

Since,  $I_C \approx I_E$  for a large  $\beta$ ,  $I_C$  is independent of  $V_C$  as long as the transistor is not saturated ( $V_C > V_E + 0.2V$ ).

**Note that the load is above the collector of the transistor and current is *sinked* through the load by the NPN transistor.**

1. **Calculate the current through the load resistor, RL(choose a RL that is less than the max. value)assuming a large  $\beta$ . Show all work. Verify your design in PSpice showing voltages and currents. To verify that your circuit is a current source independent of VS. Run a DC Sweep in PSpice from 0 to 10 volts. Determine the range of the supply voltage (VS) for a 10% current change in RL ( $I_C$ ). Print and turn in your schematic showing voltages and currents of the nodes in addition to the I-V curve with your pre-lab. VS(range) from \_\_ v to \_\_ v.**

2. Design a current source, similar to the NPN current source shown, using a PNP (2N3906) transistor. Use the same procedure as 1. above. Remember that while the NPN sinks current through the load, the PNP should source current through the load. Show all work. Determine the supply voltage as you did in 1. print and turn in your schematic showing voltages and currents of the nodes in addition to I-V curve with your pre-lab. VS(range from v to v).



**PNP Diode Current Source**

### Lab Work:

1. Perform a curve trace on an 2N2222 NPN transistor. Make a copy of your trace to be turn in with the lab.
2. Build a NPN Diode Current Source with the 2N2222 transistor and compare with design voltages and currents, PSpice voltages and currents, and measured voltages and currents.
3. Perform a DC sweep on the NPN current source from 0V to 10V. Capture the waveform on the computer to be turned in with the lab.
4. How much did the current change from between 0 and 10V ? Is this amount of change in current reasonably small, such that the design can be used as a nearly ideal current source? Why?
5. Build your PNP current source. Verify its operation. Perform a DC sweep on it from 0V to 10V and capture the waveform on the computer. Compare the PNP Current Source with your design values, PSpice values, and measured values.
6. How much did the load current( $I_{RL}$ ) change as the VS changed from 0 to 10V? At what voltage (VS) and current ( $I_{RL}$ ) did the current seem to stablies? What percentage

**DATA SHEET  
EXPERIMENT # 10**

**I.** Turn in copy of 2N2222 output characteristics curves generated by the Tektronix curve tracer.

**II. NPN Diode Current Source**

	Calculated Values	PSpice Values	Measured Values	%
$I_{RL}$				
$I_{RE}$				
$V_C$				
$V_E$				
$V_B$				

**III.** Turn in wave form

**IV.** % change (VS changed from 6 to 10 volts)

$I_{RL}$

**V. PNP Diode Current Source**

	Calculated	PSpice	Measured	%
$I_{RL}$				
$I_{RE}$				
$V_C$				
$V_D$				
$V_B$				

**VI.** % Change (Vs changed from 6 to 10 volts)

$I_{RL}$