

**ECE 2274**  
**Pre-Lab for Experiment 6**  
**555 Timer Chip**

***Introduction to the 555 Timer***

The 555 IC is a popular chip for acting as multivibrators. Go to the web to obtain a data sheet to be turn-in with the pre-lab. A simpler layout of the chip is shown below.

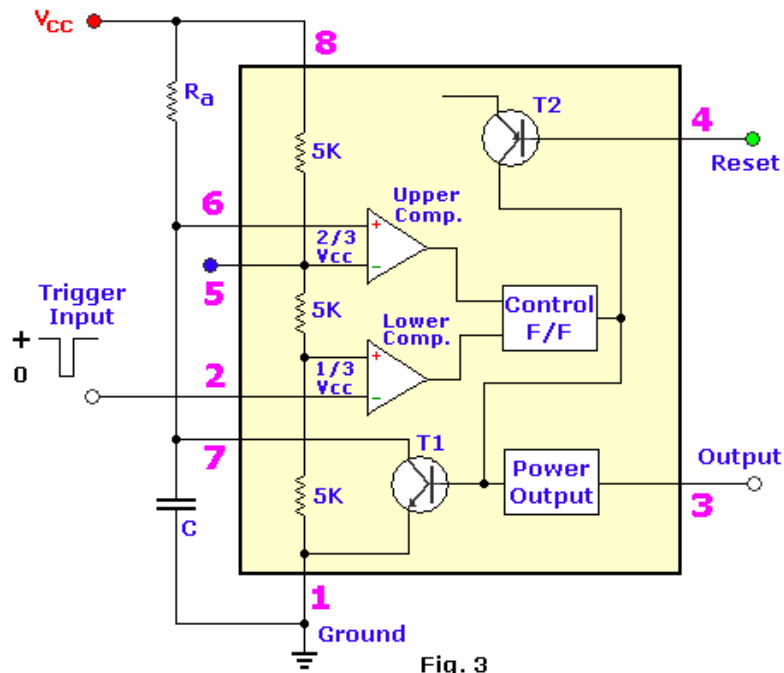


Fig. 3

*555 Timer*

**The comparators:**

The first note about the 555 timer is the comparator segments. A comparator circuit is an opamp circuit that is designed to compare an input with a fixed threshold voltage. The output will be high if the input voltage is higher, or lower depending on the comparator's design, than the threshold voltage. In the 555 IC, if the threshold pin input is higher than  $2/3V_{cc}$ , the output of CP1 goes high. When the trigger pin input is lower than  $1/3V_{cc}$ , then the output of CP2 is high.

**The RS Flip-Flop:**

The second segment of the 555 IC to analyze is the RS flip-flop. When the output of CP2 is high, and thus the output of CP1 is low, then the flip-flop has inputs,  $R=0$  and  $S=1$ . This causes the output of the RS flip-flop to be high, or logic 1. Thus, the inverted output of the flip-flop will be logic 0, or low. When the output of CP1 is high, and thus the output of CP2 is low, then the

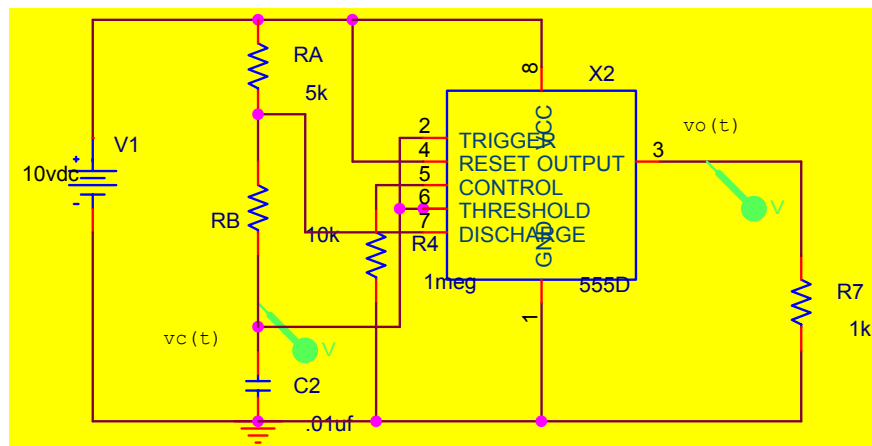
flip-flop has the inputs,  $R=1$  and  $S=0$ . This causes the output of the RS flip-flop to be logic 0 and the inverted output of the flip-flop to be logic 1. The last input pin is  $Cl$ , or reset. The reset feature of the RS flip-flop is active low. Thus, when the input to the reset pin is low, the flip-flop's output will be logic 0 and the inverted output will be logic 1. To disable the reset feature, the  $Cl$  input of the flip-flop, and thus the reset pin of the 555 IC, should be tied high.

### The Dissipation Transistor:

The last aspect of the 555 IC to be analyzed is the dissipation transistor. When the output of the flip-flop is high, and thus the inverted output is low, the transistor is off. Since, the transistor is connected to the inverted output of the flip-flop, when the inverted output is low the transistor is off because there is no current flowing in to the base of the transistor. When the output of the flip-flop is low, and thus the inverted output of the flip-flop is high, the dissipation transistor turns on and thus current flows in through the dissipation pin and to ground through the dissipation transistor.

### The 555 Astable Multivibrator

Adding two resistors and a capacitor to the 555 IC forms an astable multivibrator. An astable multivibrator is an oscillator that generates a square wave output. Build the Astable Multivibrator show below in PSpice:



*Astable Multivibrator*

Graph the output  $vo(t)$  versus the  $vc(t)$  using PSpice. The graph is to be turned in with the pre-lab.

*Using the results from your graph derive the two expressions for the period and duty cycle of the output voltage.*

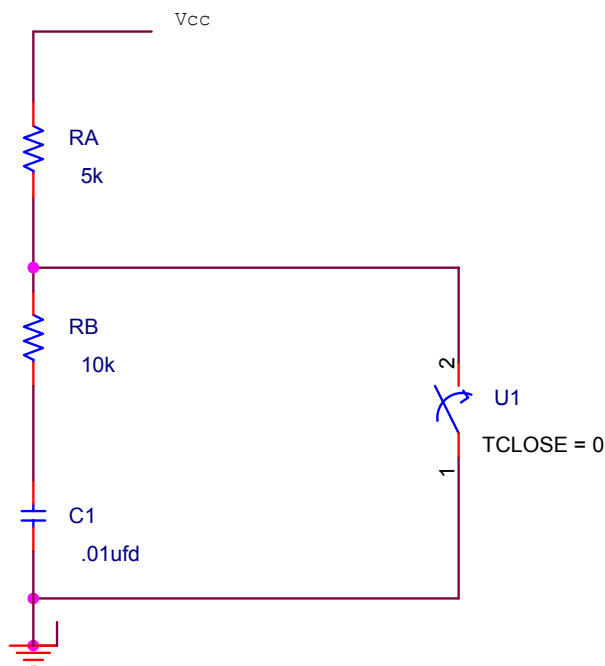
*PSpice Hint: Simulation Settings  $\Rightarrow$  Time Domain(transient)  $\Rightarrow$  Run to time 700us  $\Rightarrow$  Start saving data after 0 sec  $\Rightarrow$   $\sqrt$ Skip initial(SKIPBP)*

Using the results of the graph of output versus the capacitor, and the description of how the 555 IC works above, derive the two expressions for the period and duty cycle of the output voltage.

Hint: When the supply  $V_{cc}$  is connected, the timing capacitor  $C$  charges toward  $2/3 V_{cc}$  through  $R_A$  and  $R_B$ . When the capacitor voltage reaches  $2/3 V_{cc}$ , the upper comparator triggers the flip-flop and the capacitor starts to discharge towards ground through  $R_B$ . When the discharge reaches  $1/3 V_{cc}$ , the lower comparator is triggered and a new cycle is started.

The 555 IC can be visualized as a switch in this situation. The simplified diagram is shown below.

The switch is simulating when the discharge transistor is on and when it is off. The capacitor charges through  $R_A$  and  $R_B$  and only discharges through  $R_B$ .



**Laboratory Exercise:**

1. Build the Astable Multivibrator you used in the pre-lab. From the equations you derived determine RA and RB (C=22nf) for a output of 1kHz with a 70% duty cycle.
2. Measure your output and verify that you have obtained an output of 1kHz and 50% duty cycle. If your output does not exactly meet the specifications, explain why. Do component tolerances affect your design?
3. On channel 2 of the oscilloscope, measure the voltage across the capacitor, C. Capture and save the two output waveforms from channel 1 and 2. Overlay the captured waveforms so that both the capacitor's voltage and the output voltage are shown on the same graph. Print out only your combined graph.
4. Determine the threshold voltage of the capacitor at which the output goes low (logic 0). Then determine the trigger voltage of the capacitor at which the output goes high (logic 1).
5. Does the threshold voltage correspond reasonably well to  $2/3 V_{cc}$ ? Does the trigger voltage correspond reasonably well to  $1/3 V_{cc}$ ?
6. Build the One-Shot shown below and demonstrate how the circuit function to your lab Instructor. Do a Scope Capture to be turned-in with the lab.

